Document Number: MPXY8021A
Rev 2, 02/2006

Tire Pressure Monitoring Sensor Temperature Compensated and Calibrated, Fully Integrated, Digital Output

The Freescale Semiconductor, Inc. MPXY8021A sensor is an 8-pin tire monitoring sensor which is comprised of a variable capacitance pressure sensing element, a temperature sensing element, and an interface circuit (with a wake-up feature) all on a single chip. It is housed in a Super-Small Outline Package (SSOP), which includes a media protection filter. Specifically designed for the low power consumption requirements of tire pressure monitoring systems, it can combine with a Freescale remote keyless entry (RKE) system to facilitate a low-cost, highly integrated system.

DETAILED DESCRIPTION

The block diagram of the MPXY8021A sensor is shown in Figure 1. The pressure sensor is a capacitive transducer constructed using surface micromachining, the temperature sensor is constructed using a diffused resistor, and the interface circuit is integrated onto the same die as the sensors using a standard silicon CMOS process.

The conditioning of the pressure signal begins with a capacitance to voltage conversion (C to V) followed by a switched capacitor amplifier. This amplifier has adjustable offset and gain trimming. The offset and gain are factory calibrated, with calibration values stored in the EEPROM trim register. This amplifier also has temperature compensation circuits for both sensitivity and offset, which also are factory adjusted using the EEPROM trim register.

The pressure is monitored by a voltage comparator, which compares the measured value against an 8-bit threshold adjusted by a serial input. By adjusting the threshold and monitoring the state of the OUT pin the external device can check whether a low-pressure threshold has been crossed, or perform up to 8-bit A/D conversions.

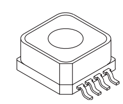
The temperature is measured by a diffused resistor with a positive temperature coefficient driven by a current source, thereby creating a voltage. The room temperature value of this voltage is factory calibrated using the EEPROM trim register. A two-channel multiplexer can route either the pressure or temperature signal to a sampling capacitor that is monitored by a voltage comparator with variable threshold adjust, providing a digital output for temperature.

An internal low frequency, low power 5.4 kHz oscillator with a 14-stage divider provides a periodic pulse to the OUT pin (divide by 16384 for 3 seconds). This pulse can be used to wake up an external MCU to begin an interface with the device. An additional 10-stage divider will provide a pulse every 52 minutes which can be used to reset an external MCU.

The power consumption can be controlled by several operational modes selected by external pins.

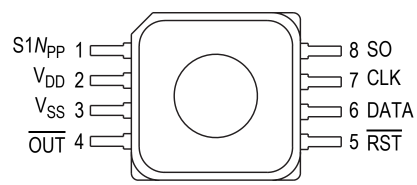
MPXY8021A

TIRE PRESSURE MONITORING SENSOR MPXY8021A: OPTIMIZED FOR 250 kPA – 450 kPA



SUPER SMALL OUTLINE PACKAGE CASE 1352-03

PIN ASSIGNMENT



8-pin Super Small Outline Package (SSOP)

ORDERING INFORMATION	
Shipped in Rails	**Shipped in Tape & Reel**
MPXY8021A6U	MPXY8021A6T1

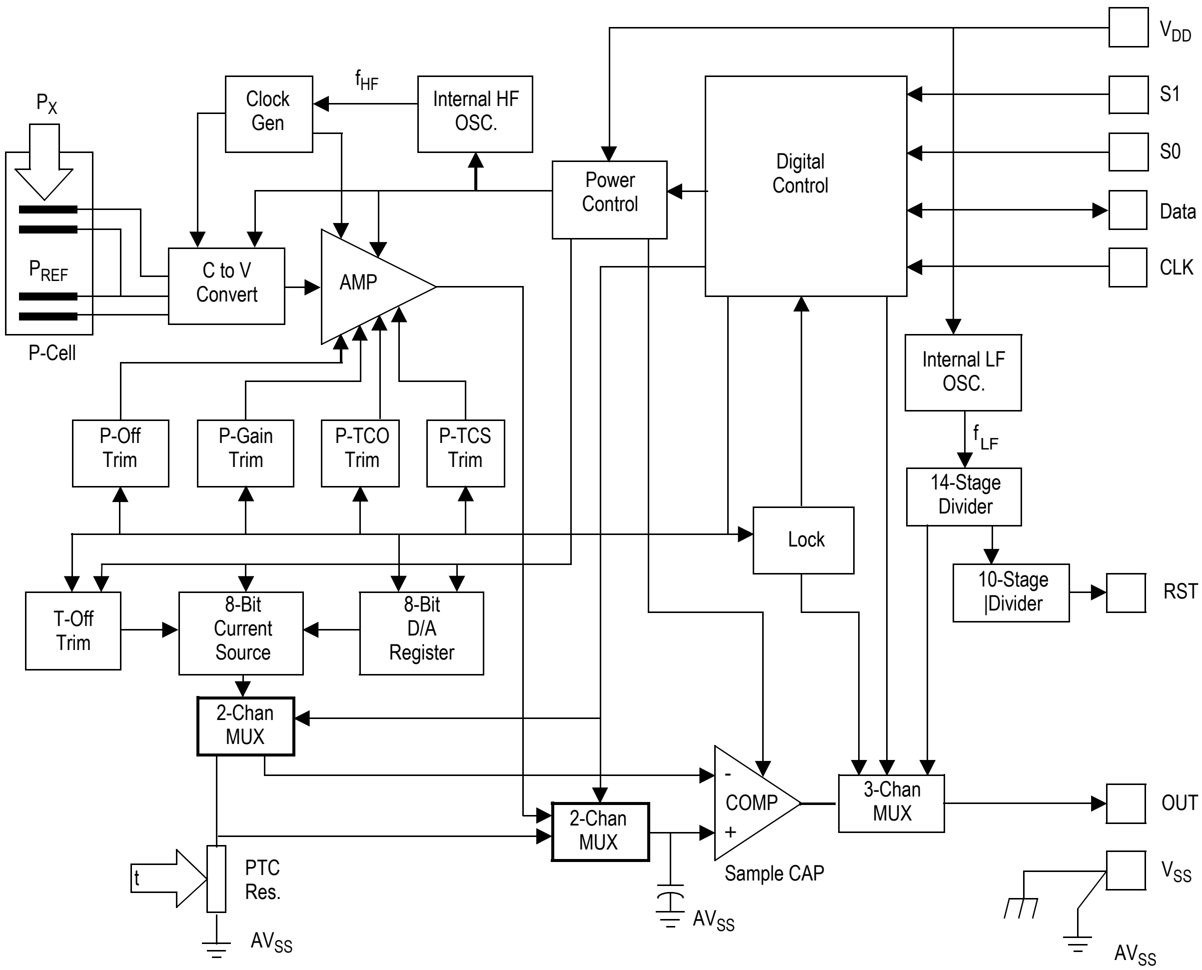


Figure 1. MPXY8021A Sensor Block Diagram

OPERATING MODES

The device has several operating modes dependent on the applied voltages to the S1 and S0 pins as shown in Table 1. In all the modes listed the channel multiplexers, D/A Register, LFO, and the output pulse dividers will always be powered up as long as there is a voltage source connected to the V_{DD} pin.

When only the S0 pin is at a logic one the pressure measuring circuit in the device is powered up and the pressure output signal is connected to the sample capacitor through a multiplexer. When the S0 pin returns to the low state the multiplexer will first turn off to store the signal on the sample capacitor before powering down the measuring circuitry.

When only the S1 pin is at a logic one the temperature measuring circuit in the device is powered up and the temperature output signal is connected to the sample capacitor through a multiplexer. When the S1 pin returns to the low state the multiplexer will first turn off to store the signal on the sample capacitor before powering down the measuring circuitry.

NOTE: All of the EEPROM trim bits will be powered up regardless of whether the pressure or temperature measuring circuitry is activated.

NOTE: If the voltage on the S1 pin exceeds 2.5 times the voltage on the V_{DD} pin the device will be placed into its Trim/Test Mode.

NOTE: If the V_{DD} supply source is switched off in order to reduce current consumption, it is important that all input pins be driven LOW to avoid powering up the device.

If any input pin (S1, S0, DATA, or CLK) is driven HIGH while the V_{DD} supply is switched off, the device may be powered up through an ESD protection diode. Such a case should be avoided. The effective source voltage of the device will be less than the applied voltage due to diode voltage drop. In addition, the entire source current will be drawn from the input pin.

Table 1. Operating Modes

S1	S0	Operating Mode	Circuitry Powered				Serial Data Counter
			Pressure Measure System	Temp Measure System	A/D Output Comp.	LFO Oscill.	
0	0	Standby/Reset	OFF	OFF	OFF	ON	ACTIVE
0	1	Measure Pressure	ON	OFF	OFF	ON	RESET
1	0	Measure Temperature	OFF	ON	OFF	ON	RESET
1	1	Output Read	OFF	OFF	ON	ON	ACTIVE

PIN FUNCTIONS

The following paragraphs give a description of the general function of each pin.

V_{DD} and V_{SS} Pins

Power is supplied to the control IC through V_{DD} and V_{SS}. V_{DD} is the positive supply and V_{SS} is the digital and analog ground. The control IC operates from a single power supply. Therefore, the conductors to the power supply should be connected to the V_{DD} and V_{SS} pins and locally decoupled as shown in Figure 2.

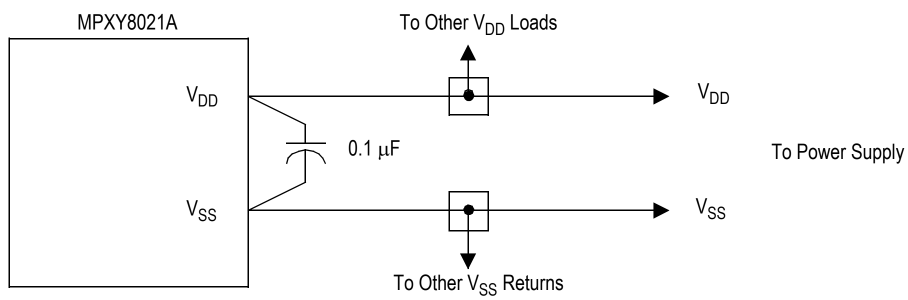


Figure 2. Recommended Power Supply Connections

OUT Pin

The OUT pin normally provides a digital signal related to the voltage applied to the voltage comparator and the threshold level shifted into an 8-bit register from an external device. When the device is placed in the standby mode the OUT pin is driven high and will be clocked low when an overflow is detected from a clock divider (divide by 16384) driven by the LFO. This allows the OUT pin to wake up an external device such as an MCU.

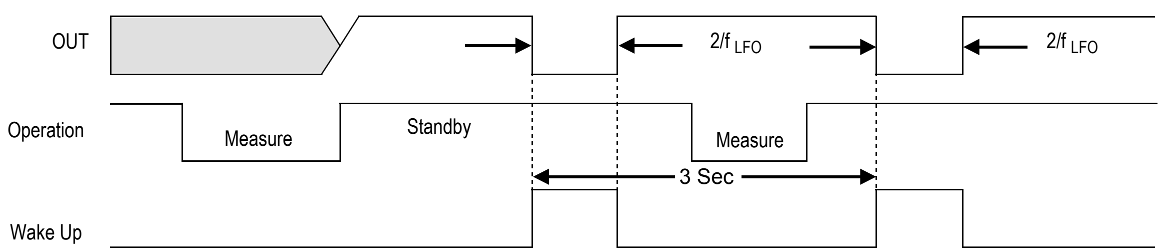


Figure 3. Pulse on OUT Pin During Standby Mode

$\overline{\text{RST}}$ Pin

The $\overline{\text{RST}}$ pin is normally driven high and will be clocked low when an overflow is detected from total clock divider (divide by 16,777,216) driven by the LFO. This allows the $\overline{\text{RST}}$ pin to reset an external device such as an MCU. This pulse will appear on the $\overline{\text{RST}}$ pin approximately every 52 minutes regardless of the operating mode of the device. The pulse lasts for two cycles of the LFO oscillator as shown in Figure 4. Since the RST pin is clocked from the same divider string as the $\overline{\text{OUT}}$ pin, there will also be a pulse on the OUT pin when the $\overline{\text{RST}}$ pin pulses every 52 minutes.

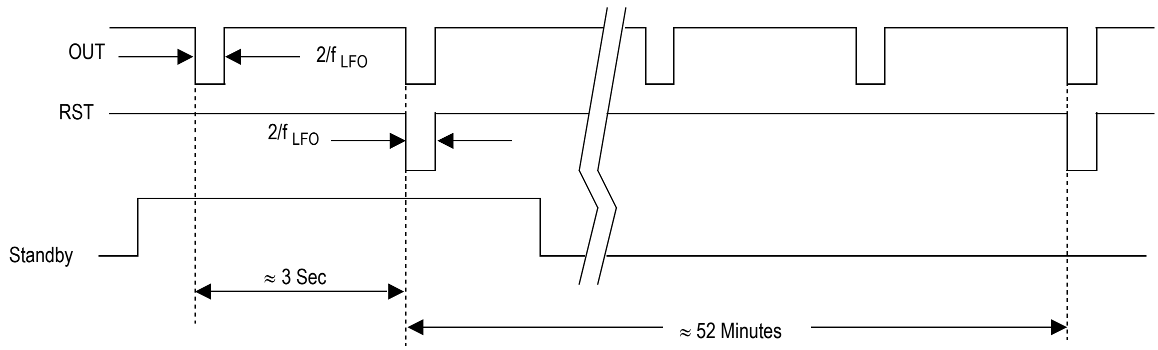


Figure 4. Pulse on $\overline{\text{RST}}$ Pin

S0 Pin

The S0 pin is used to select the mode of operation as shown in Table 1.

The S0 pin contains an internal Schmitt trigger as part of its input to improve noise immunity. The S0 pin has an internal pull-down device in order to provide a low level when the pin is left unconnected.

S1 Pin

The S1 pin is used to select the mode of operation, as shown in Table 1.

The S1 pin contains an internal Schmitt trigger as part of its input to improve noise immunity. This pin has an internal pull-down device to provide a low level when the pin is left unconnected.

The S1 pin also serves the purpose of enabling factory trim and test of the device.

The higher V_{PP} programming voltage for the internal EEPROM trim register is also supplied through the S1 pin.

DATA Pin

The DATA pin is the serial data in (SDI) function for setting the threshold of the voltage comparator.

The DATA pin contains an internal Schmitt trigger as part of its input to improve noise immunity. This pin has an internal pull-down device to provide a low level when the pin is left unconnected.

CLK Pin

The CLK pin is used to provide a clock used for loading and shifting data into the DATA pin. The data on the DATA pin is clocked into a shift register on the rising edge of the CLK pin signal. The data is transferred to the D/A Register on the eighth falling edge of the CLK pin. This protocol may be handled by the SPI or SIOP serial I/O function found on some MCU devices.

The CLK pin contains an internal Schmitt trigger as part of its input to improve noise immunity. The CLK pin has an internal pull-down device to provide a low level when the pin is left unconnected.

Output Threshold Adjust

The state of the OUT pin is driven by a voltage comparator whose output state depends on the level of the input voltage on the sample capacitor and the level of an adjustable 8-bit threshold voltage. The threshold is adjusted by shifting data bits into the D/A Register (DAR) via the DATA pin while clocking the CLK pin. The timing of this data is shown in Figure 5. Data is transferred into the serial shift register on the rising edge of the CLK pin. On the falling edge of the 8^{th} clock the data in the serial shift register is latched into the parallel DAR register. The DAR remains powered up whenever V_{DD} is present. The serial data is clocked into the DATA pin starting with the MSB first. This sequence of threshold select bits is shown in Table 2.

Table 2. D/A Threshold Bit Assignment

Function		Bit Weight	Data Bit
Voltage Comparator Threshold Adjust (8 bits)	LSB	1	D0
		2	D1
		4	D2
		8	D3
		16	D4
		32	D5
		64	D6
	MSB	128	D7

An analog to digital (A/D) conversion can be accomplished with eight (8) different threshold levels in a successive approximation algorithm; or the OUT pin can be set to trip at some alarm level. The voltage on the sample capacitor will maintain long enough for a single 8-bit conversion, but may need to be refreshed with a new measured reading if the read interval is longer than the specified hold time, t_{SH}.

The counter that determines the number of clock pulses into the device is reset whenever the device is placed into the Measure Pressure or Measure Temperature Modes. This provides a means to reset the data transfer count in case the clock stream is corrupted during a transmission. In these two modes the DATA and CLK pins should not be clocked to reduce noise in the captured pressure or temperature data. Any change in the DAR contents should be done during the Standby or Output Read Modes.

Both the serial bit counter and the state of the DAR are undefined following power up of the device. The serial bit counter can be reset by cycling either the SO pin or the S1/VPP pin to a high level and then back low. The DAR can then be reset to the lowest level by holding the DATA pin low while bursting the CLK pin with eight (8) clock pulses.

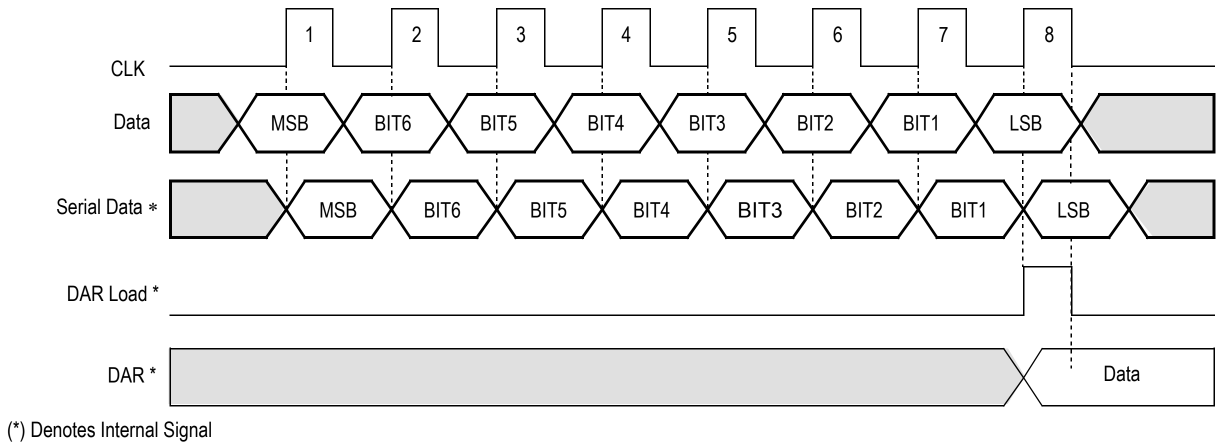


Figure 5. Serial Data Timing

Pressure Sensor Output

The pressure channel compares the output of its analog measurement circuit to the D/A reference voltage. The device is calibrated at two different nominal values depending on the calibration option.

Temperature Sensor Output

The temperature channel compares the output of a positive temperature coefficient (PTC) resistor driven by a switched current source. The current source is only active when the temperature channel is selected.

APPLICATIONS

Suggested application example is shown in Figure 6.

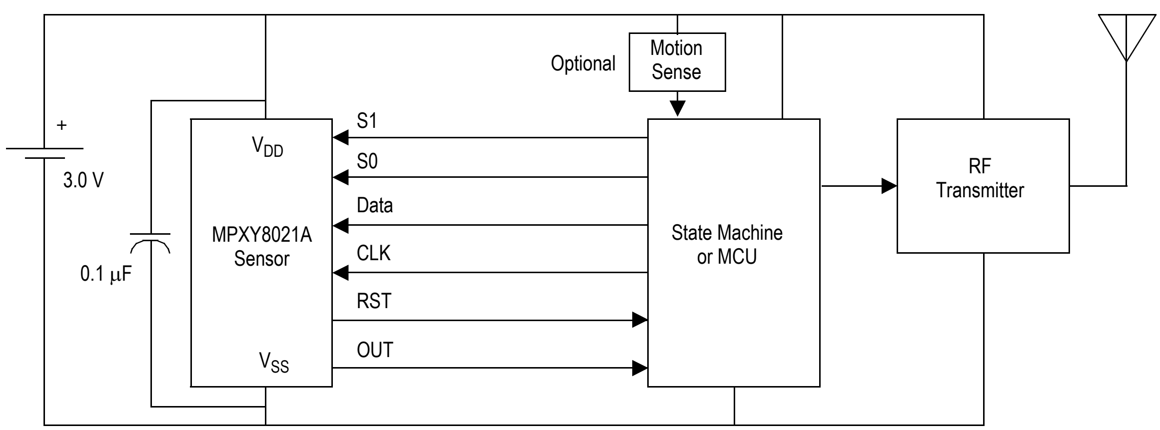


Figure 6. Application Example

ELECTRICAL SPECIFICATIONS

Maximum ratings are the extreme limits to which the device can be exposed without permanently damaging it. The device contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table below. Keep V_{IN} and V_{OUT} within the range $V_{SS} \leq (V_{IN}$ or $V_{OUT}) \leq V_{DD}$.

Table 3. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 to +4.0	V
Short Circuit Capability (all pins excluding V_{DD} and V_{SS}) Maximum High Voltage for 5 minutes Minimum Low Voltage for 5 minutes	 V_{SC} V_{SC}	 V_{DD} V_{SS}	 V V
Substrate Current Injection Current from any pin to V_{SS} –0.3 VDC)	 I_{SUB}	 600	 µA
Electrostatic Discharge Human Body Model (HBM) Charged Device Model (CDM) Machine Model (MM)	 V_{ESD} V_{ESD} V_{ESD}	 ±1000 ±1000 ±200	 V V V
Storage Temperature Range Standard Temperature Range	 T_{stg}	 –40 to +150	 °C

Table 4. Operating Range

The limits normally expected in the application which define range of operation.

Characteristic	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{DD}	2.1	3.0	3.3	V
Operating Temperature Range Standard Temperature Range	 T_A	T_L –40	 —	T_H +125	 °C
Pressure Operating Range MPXY8021A	 $P_{637.5}$	 50	 —	 637.5	 kPa
Supply Current Drain Standby Mode –40°C to +85°C +85°C to +100°C +100°C to +125°C	 I_{STBY} I_{STBY} I_{STBY}	 — — —	 0.6 0.8 1.5	 0.9 1.2 2.2	 µA µA µA
Read Mode –40°C to +125°C	 I_{READ}	 —	 400	 600	 µA
Measure Temperature Mode –40°C to +125°C	 I_{TEMP}	 —	 400	 600	 µA
Measure Pressure Mode –40°C to +10°C +10°C to +60°C +60°C to +125°C	 I_{PRESS} I_{PRESS} I_{PRESS}	 — — —	 1400 1300 1200	 1800 1700 1700	 µA µA µA

Table 5. Electrical Characteristics

+2.1 V ≤ V_{DD} ≤ +3.6 V, T_L ≤ T_A ≤ T_H, unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Units
Output High Voltage DATA, OUT, $\overline{RST}$ (I_{Load} = 100 μA)	V_{OH}	V_{DD} –0.8	—	—	V
Output Low Voltage DATA, OUT, $\overline{RST}$ (I_{Load} = -100 μA)	V_{OL}	—	—	0.4	V
Input High Voltage S0, S1, DATA, CLK	V_{IH}	0.7 x V_{DD}	—	—	V
Input Low Voltage S0, S1, DATA, CLK	V_{IL}	V_{SS}	—	0.3 x V_{DD}	V
Input Hysteresis (V_{IH} — V_{IL}) S0, S1, DATA, CLK	V_{HYS}	100	200	—	mV
Input Low Current (at V_{IL}) S0, S1, DATA, CLK	I_{IL}	-5	-25	-100	μA
Input High Current (at V_{IH}) S0, S1, DATA, CLK	I_{IH}	-5	-35	-140	μA (2)
Temperature Measurement (+2.1 V ≤ V_{DD} < +2.5 V) D/A Conversion Code at -40°C D/A Conversion Code at -20°C D/A Conversion Code at 25°C D/A Conversion Code at 70°C D/A Conversion Code at 100°C D/A Conversion Code at 120°C D/A Conversion Code at 125°C	 T_{-40} T_{-20} T_{25} T_{70} T_{100} T_{120} T_{125}	 34 52 97 154 203 240 249	 42 57 102 163 214 252 255	 51 67 107 172 225 255 255	 counts counts counts counts counts counts counts
Temperature Measurement (+2.5 V ≤ V_{DD} ≤ +3.0 V) D/A Conversion Code at -40°C D/A Conversion Code at -20°C D/A Conversion Code at 25°C D/A Conversion Code at 70°C D/A Conversion Code at 100°C D/A Conversion Code at 120°C D/A Conversion Code at 125°C	 T_{-40} T_{-20} T_{25} T_{70} T_{100} T_{120} T_{125}	 36 52 97 155 204 241 249	 42 57 102 163 214 252 255	 50 64 107 171 224 255 255	 counts counts counts counts counts counts counts
Temperature Measurement (+3.0 V < V_{DD} ≤ +3.6 V) D/A Conversion Code at -40°C D/A Conversion Code at -20°C D/A Conversion Code at 25°C D/A Conversion Code at 70°C D/A Conversion Code at 100°C D/A Conversion Code at 120°C D/A Conversion Code at 125°C	 T_{-40} T_{-20} T_{25} T_{70} T_{100} T_{120} T_{125}	 36 52 97 154 203 240 249	 42 57 102 163 214 252 255	 49 64 107 172 225 255 255	 counts counts counts counts counts counts counts
Temperature Sensitivity at 25°C		—	0.80		°C/bit
Approximate Temperature Output Response	OUT = 74.75 + 0.075 x Ta + 0.0041 x Ta^2				counts

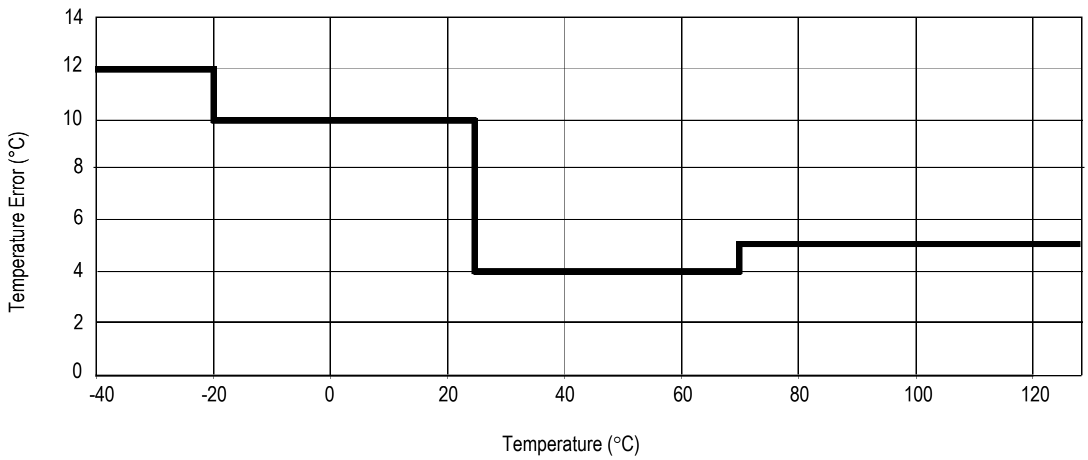


Figure 7. Temperature Error vs Temperature at V_{DD} = 3.0 V

Table 6. Control Timing
+2.1 V ≤ V_{DD} ≤ +3.6 V, $T_L \le T_A \le T_H$, unless otherwise specified.

Characteristic	Symbol	Min	Typ	Max	Units
HFO Measurement Clock Frequency	f_{HF}	100	135	150	kHz
LFO Wake Up Clock Frequency Ta = –40°C, +2.1 V ≤ V_{DD} ≤ +3.6 Ta = +25°C, +2.1 V ≤ V_{DD} ≤ +3.6 Ta = +125°C, +2.1 V ≤ V_{DD} ≤ +3.6	 f_{LF} f_{LF} f_{LF}	 3300 3900 3800	 5400 5400 5300	 8000 7700 7000	 Hz Hz Hz
Wake Up Pulse Pulse Timing Pulse Width	 t_{WAKE} t_{WPW}	 — —	 16384 2	 — —	 LFO clocks LFO clocks
Reset Pulse Pulse Timing Pulse Width	 t_{RESET} t_{RPW}	 — —	 16,777,216 2	 — —	 LFO clocks LFO clocks
Minimum Setup Time (DATA edge to CLK rise)	t_{SETUP}	100	—	—	nSec
Minimum Hold Time (CLK rise to DATA change)	t_{HOLD}	100	—	—	nSec
Measurement Response Time Recommended time to hold device in measurement mode Temperature Pressure	 t_{TMEAS} t_{PMEAS}	 — —	 200 500	 — —	 µSec µSec
Read Response Time (see Figure 8) From 90% V_{DD} on S0 to OUT less than V_{OL} or greater than V_{OH}	 t_{READ}	 —	 50	 100	 µSec
Sample Capacitor Discharge Time From initial full scale D/A count (255) to drop 2 counts (253)	 t_{SH}	 20	 —	 —	 mSec

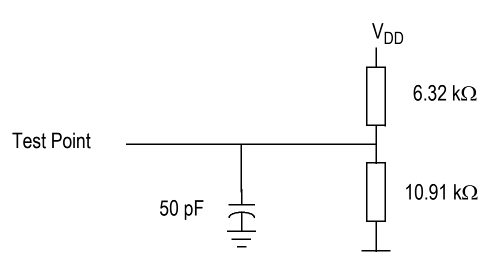


Figure 8. Control Timing Test Load for OUT and $\overline{RST}$ Pins

SENSOR CHARACTERISTICS (MPXY8021A)

PRESSURE TRANSFER FUNCTION

kPa = 2.5 x Output ± (Pressure Error)
Output = 8-bit digital pressure measurement (between 0-255)

Pressure Error (±kPa): 50 kPa ≤ P < 250 kPa

T[°C] \ V_{DD}[V]	2.1	2.5	2.7	3.0	3.3	3.6
–40	72.5	72.5	35.0	35.0	35.0	37.5
–20	57.5	57.5	30.0	30.0	30.0	35.0
0	57.5	57.5	25.0	25.0	25.0	27.5
25	57.5	57.5	25.0	25.0	25.0	27.5
70	57.5	57.5	27.5	25.0	25.0	27.5
100	72.5	72.5	37.5	37.5	37.5	37.5
125	95.0	92.5	57.5	47.5	47.5	47.5

Pressure Error (±kPa): 250 kPa ≤ P ≤ 450 kPa

T[°C] \ V_{DD}[V]	2.1	2.5	2.7	3.0	3.3	3.6
–40	40.0	40.0	30.0	30.0	30.0	35.0
–20	32.5	25.0	20.0	20.0	20.0	25.0
0	30.0	25.0	10.0	10.0	10.0	15.0
25	30.0	25.0	7.5	7.5	7.5	15.0
70	35.0	25.0	10.0	7.5	7.5	15.0
100	40.0	40.0	25.0	25.0	25.0	30.0
125	62.5	60.0	35.0	35.0	35.0	35.0

Pressure Error (±kPa): 450 kPa < P ≤ 637.5 kPa

T[°C] \ V_{DD}[V]	2.1	2.5	2.7	3.0	3.3	3.6
–40	70.0	70.0	40.0	40.0	40.0	40.0
–20	55.0	55.0	30.0	30.0	30.0	35.0
0	55.0	55.0	22.5	22.5	22.5	35.0
25	55.0	55.0	22.5	22.5	22.5	35.0
70	55.0	55.0	25.0	25.0	25.0	35.0
100	70.0	70.0	32.5	32.5	32.5	40.0
125	90.0	90.0	47.5	47.5	47.5	52.5

Areas marked in grey indicate the typical operating range.

PRESSURE ERROR

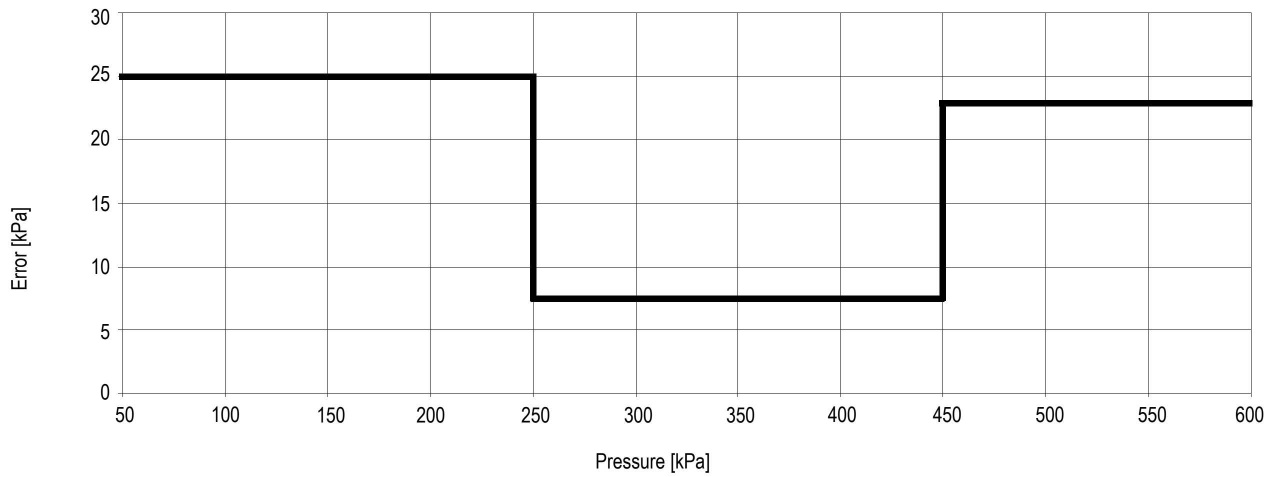


Figure 9. Pressure Error vs Pressure at T = 25°C, 2.7 V ≤ V_{DD} ≤ 3.3 V

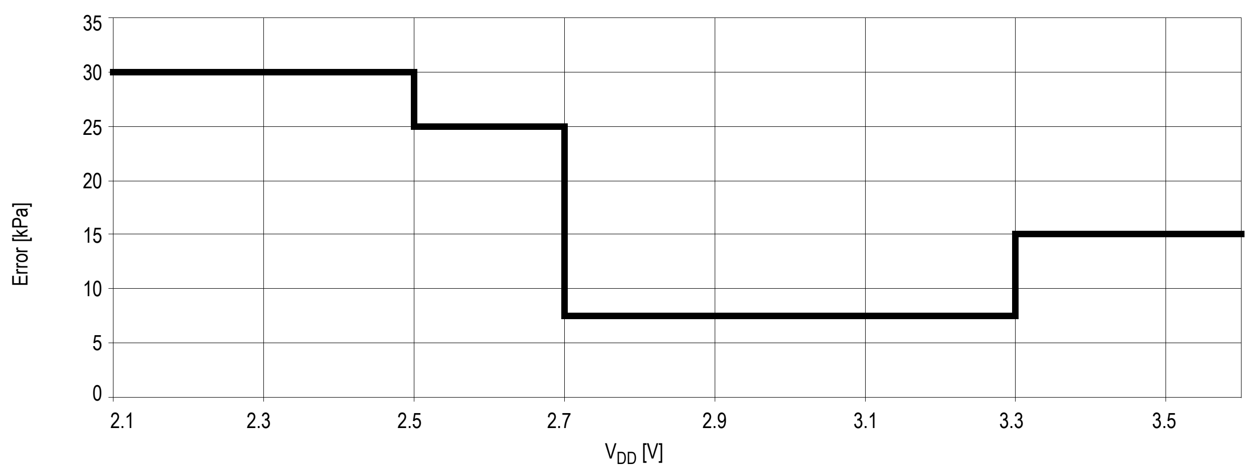


Figure 10. Pressure Error vs V_{DD} at T = 25°C, 250 kPa ≤ P ≤ 450 kPa

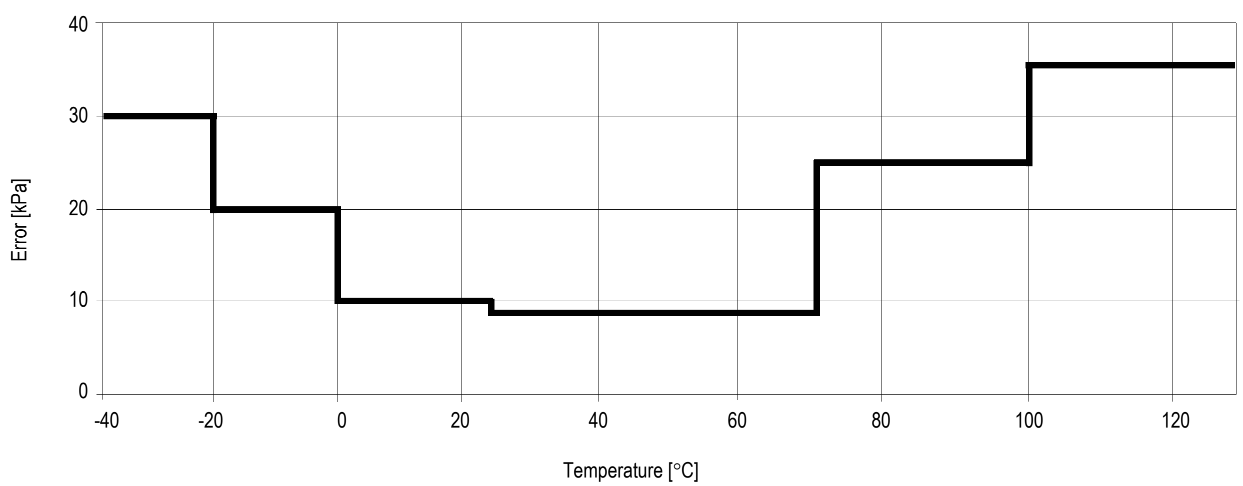


Figure 11. Pressure Error vs Temperature at V_{DD} = 3.0 V, 250 kPa ≤ P ≤ 450 kPa

MECHANICAL SPECIFICATIONS

Maximum ratings are the extreme limits to which the device can be exposed without permanently damaging it.

Keep V_{IN} and V_{OUT} within the range $V_{SS} \leq (V_{IN}$ or $V_{OUT}) \leq V_{DD}$.

Table 7. Maximum Ratings

Rating	Symbol	Value	Unit
Maximum Pressure[1]	p_{max}	1400	kPa[1]
Centrifugal Force Effects (3 axis) Pressure measurement change less than 1% FSS	g_{CENT}	2000	g
Unpowered Shock (three sides, 0.5 mSec duration)	g_{shock}	2000	g

1. Tested for 5 minutes at 25°C.

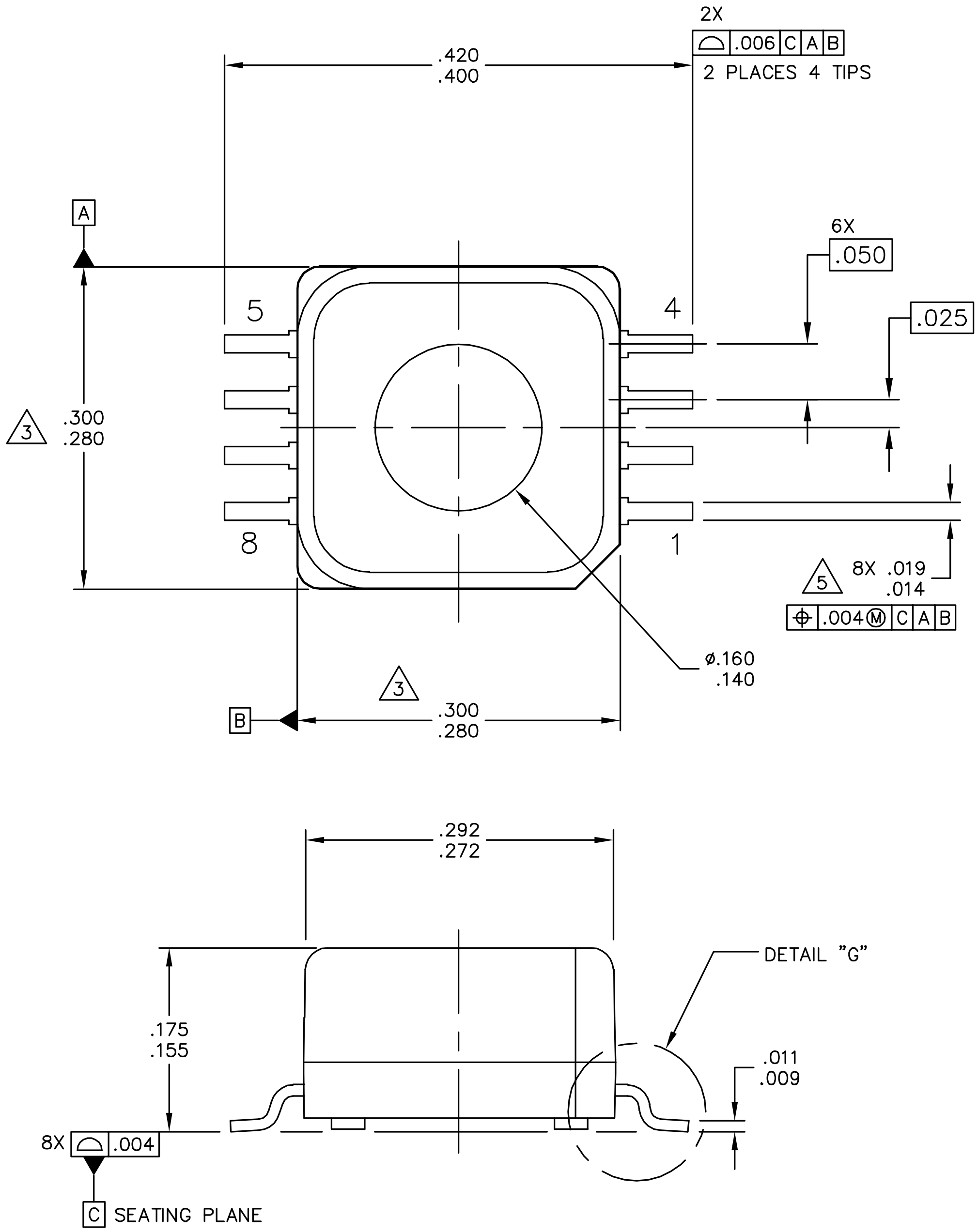
MEDIA COMPATIBILITY

The Daytona sensor has been designed with the tire pressure application in mind. As such, it has been tested to a variety of media typical of the tire environment. The filter provides limited, but not universal, media protection.

The customer must ensure media compatibility of the Daytona sensor in their application. In particular, it is strongly recommended that the customer design the application such that media does not come in direct contact with the sensor. Module housing design and orientation will play a role in protecting the sensor from direct media exposure. In the event that media does come in contact with the sensor it is desirable that the application minimize the duration and severity of exposure. Media may be forced through the filter by mechanical aspects of the application such as g-forces or rapid pressurization of the tire.

In addition, the customer maintains responsibility to design and carry out reliability testing verifying compatibility of the Daytona sensor with their module design and application.

PACKAGE DIMENSIONS



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TITLE: 8 LEAD TPMP GULL WING FORM	DOCUMENT NO: 98ASA99256D	REV: C
	CASE NUMBER: 1352–03	24 JUL 2005
	STANDARD: NON–JEDEC	

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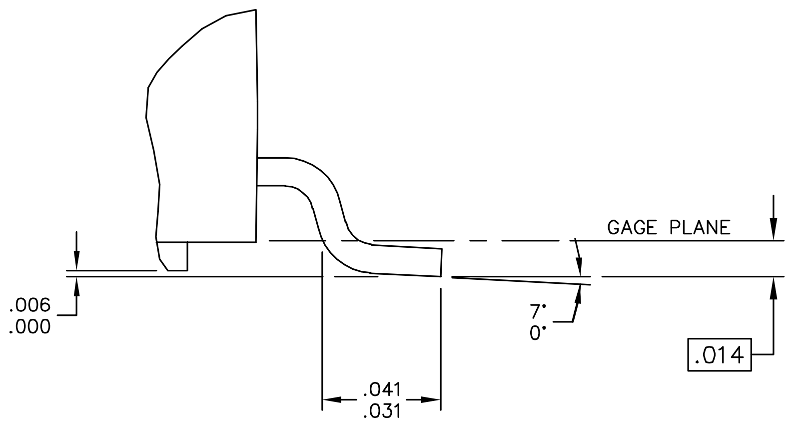
CASE 1352-03
ISSUE C
SUPER SMALL OUTLINE PACKAGE

PACKAGE DIMENSIONS



DETAIL "G"

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TITLE: 8 LEAD TPMP GULL WING FORM	DOCUMENT NO: 98ASA99256D	REV: C
	CASE NUMBER: 1352–03	24 JUL 2005
	STANDARD: NON–JEDEC	

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CASE 1352-03
ISSUE C
SUPER SMALL OUTLINE PACKAGE

PACKAGE DIMENSIONS

NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.
3. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FALSH AND PRPTRUSIONS SHALL NOT EXCEED .006 PER SIDE.
4. ALL VERTICAL SURFACES TO BE 5° MAXIMUM.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 MAX.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 8 LEAD TPMP GULL WING FORM	DOCUMENT NO: 98ASA99256D		REV: C
	CASE NUMBER: 1352−03		24 JUL 2005
	STANDARD: NON−JEDEC		

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CASE 1352-03
ISSUE C
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