# [MG2471] Datasheet

**(No. ADS0901)**

**V1.2**

# REVISION HISTORY

| Version | Date | Description |
|---|---|---|
| V1.0 | 2014.3.27 | ▪ The first version release. |
| V1.1 | 2014.5.9 | ▪ Updated Sec 8.15<br>▪ Unified the abbreviations for Write-Only and Read-Only (WO: Write-Only, RO: Read-Only) |
| V1.2 | 2014.9.1 | ▪ Updated Sec 5.8, Crystal Oscillator parameters (TYP and MAX value for ESR, $C_O$ and $C_L$) are updated.<br>▪ Table 3. Bill of Materials in Sec. 6 is updated. $C_{11}$ and $C_{12}$ is changed from 30pF to 13pF. |

# CONTENTS

# FIGURES

# TABLES

# 1. INTRODUCTION

**MG2471** is a true 2.4 GHz system-on-chip (SOC) designed for low-power and low-cost applications based on IEEE802.15.4 and RF4CE. The MG2471 uses the ISM band of 2.4 ~ 2.48 GHz. In addition to the standard data-rate specified in IEEE802.15.4, enhanced multiple data-rate modes (31.25Kbps ~ 1Mbps) with channel coding are supported.

**MG2471** combines an advanced RF transceiver with an industry-standard enhanced 8051 MCU, a baseband PHY, a MAC with AES-128 HW engine, an in-system programmable 64KB flash memory, a 6-KB RAM, and many other application-specific peripherals.
This chip is best for very low-power RF4CE remote control applications.

## 1.1. APPLICATIONS

- 2.4 GHz IEEE 802.15.4 Applications
- RF4CE Remote Control Systems
- Lighting Systems
- Home/Building Automation
- Industrial Control and Monitoring
- Energy Management
- Low Power Wireless Sensor Networks
- Consumer Electronics
- Health-care equipment
- Toys

# 2. KEY FEATURES

**RF Transceiver**

- Single-chip 2.4GHz RF Transceiver
- Low Power Consumption
- High Sensitivity of –98dBm at 250kbps
- No External T/R Switch or Filter needed
- On-chip VCO, LNA, and PA
- Programmable Output Power up to +9.0dBm
- Direct Sequence Spread Spectrum
- O-QPSK Modulation
- Scalable Data Rate including 250Kbps specified in IEEE802.15.4: 31.25Kbps ~ 1Mbps
- RSSI Measurement
- Compliant to IEEE802.15.4

**Hardwired MAC**

- Two 256-byte circular FIFOs
- FIFO management
- AES Encryption/Decryption Engine(128 bit)
- CRC-16 Computation and Check

**8051-Compatible MCU**

- 8051 Compatible (single cycle execution)
- 64KB Embedded Flash Memory
- 6KB Data Memory
- 128-byte CPU dedicated Memory
- 1KB Boot ROM
- Dual DPTR Support
- I2S/PCM Interface with two 256-byte FIFOs
- Two High-Speed UARTs with Two 16-byte FIFOs(up to 1Mbps)
- Four Timer/Counters
- 5 PWM channels
- Watchdog Timer
- Sleep Timer using the 32kHz RC-OSC clock
- Quadrature Signal Decoder
- 22 General Purpose I/Os
- Internal 32kHz RC oscillator for Sleep Timer
- 16 MHz RC oscillator for the fast start-up from reset & power-down mode
- On-chip Power-on-Reset and Brown-out detector
- 4-channel 12-bit ADC( ENOB > 10-bit)
- SPI Master/Slave Interface with two 16-byte FIFOs
- I2C Master/Slave with 16-byte FIFO
- Programmable IR(Infra-Red) Modulator
- ISP (In System Programming)
- External clock output function(500KHz, 1/2/4/8/16/32 MHz selectable)

**Clock Inputs**

- 32MHz Crystal for System Clock

**Power**

- 1.8V(Core)/2.0~3.6V(I/O) Operation
- Power Management Scheme with Deep Sleep Mode
- Separate On-chip Regulators for Analog and Digital Circuitry.
- Power Supply Range for Internal Regulator(2.0V(Min) ~ 3.6V(Max))

**Package**

- Lead-Free 48-pin QFN Package (7mm x 7mm)

# 3. BLOCK DIAGRAM

[Figure 1] shows the block diagram of MG2471. The MG2471 consists of a 2.4GHz RF, a baseband PHY, a MAC hardware engine, an industry-standard enhanced 8051 MCU, an in-system programmable flash memory 64KB, a 6KB data RAM, and rich peripherals such as I2C, 5-channel PWM.

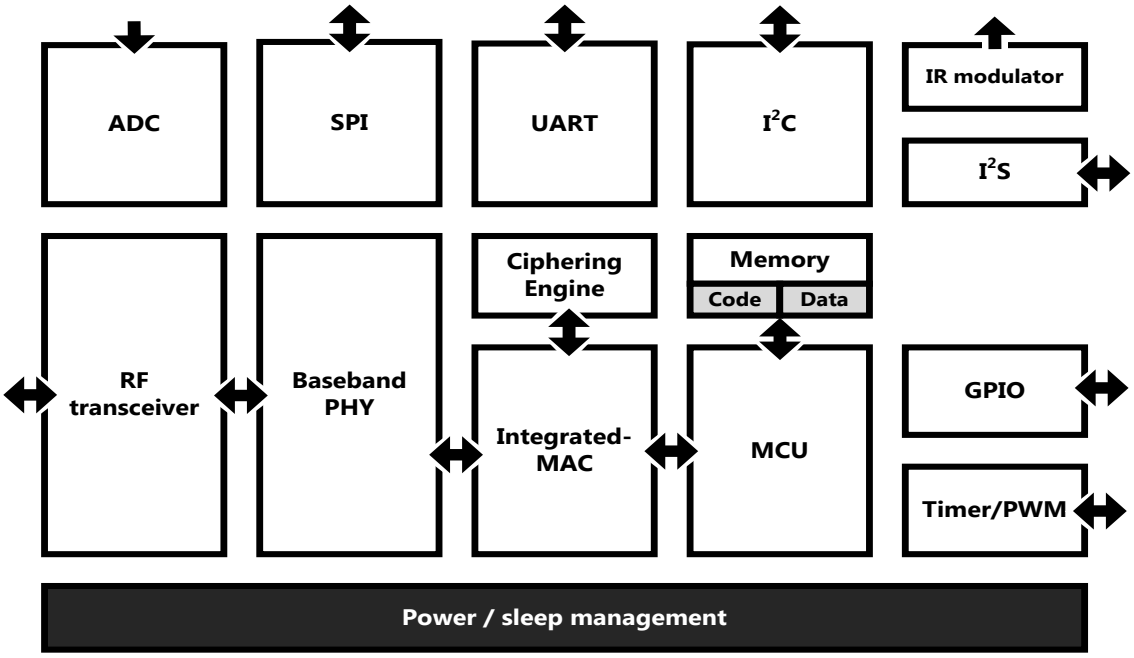



**Figure 1. Functional Block Diagram of MG2471**

MG2471 integrates an RF transceiver compliant to IEEE802.15.4 RF. The RF transceiver operates on an ISM band of 2.4 ~ 2.48GHz with excellent receiver sensitivity and programmable output power up to +8.8dBm.

The MAC block supports IEEE802.15.4 compliant functions and it is located between the microprocessor and the baseband modem. MAC block includes FIFOs for transmitting/receiving packets, an AES engine for security operation, a CRC and related control circuit. In addition, it supports automatic CRC check and address decoding.

MG2471 integrates a high performance embedded microcontroller, compatible to industry standard 8051 microcontroller in an instruction level. This embedded microcontroller has 8-bit operation architecture sufficient for controller applications. The embedded microcontroller has 4-stage pipeline architecture to improve the performance over previous compatible chips making it capable of executing simple instructions during a single cycle.

The memory part of the embedded microcontroller consists of program memory and data memory. The data memory has 2 memory areas. For more detailed explanations, refer to Sec 7.1.2. Data Memory.

MG2471 includes 22 GPIOs and various peripheral circuits to aid in the development of the application circuit with an interrupt handler to control the peripherals. MG2471 uses 32MHz

crystal oscillator for RF PLL and 8MHz clock generated from 32MHz in clock generator is used as the default clock of 8051 MCU subsystem. The clocks for MAC, a baseband modem are separately controlled by the internal clock and reset block.

# 4. PIN DESCRIPTION

The pin-out diagram of MG2471 is shown in [Figure 2] and the detailed description is in [Table 1].

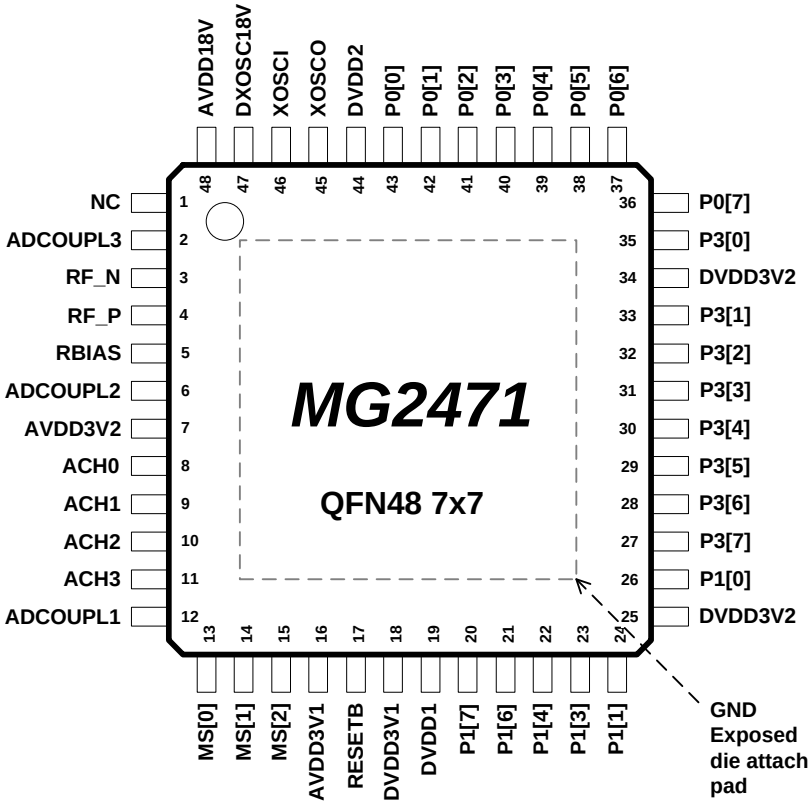



**Figure 2. Pinout Top View of MG2471**

**Note:** The exposed ground pad is located at the bottom of the chip and electrically connected to the die ground inside the package. It must be connected to a solid ground plane.

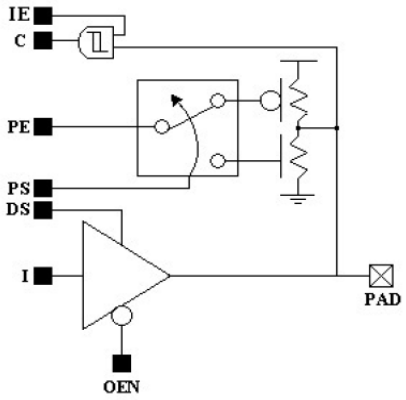
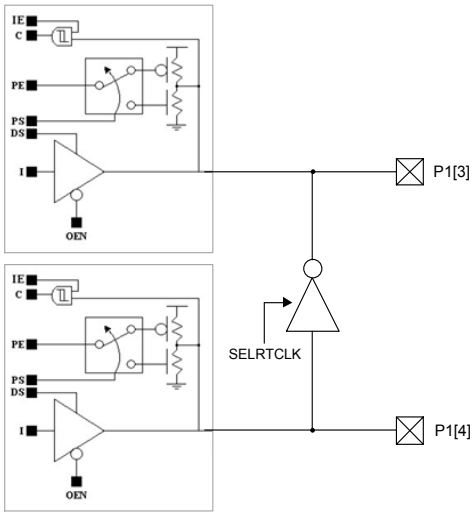
**Table 1. Pin Description**

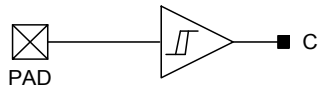
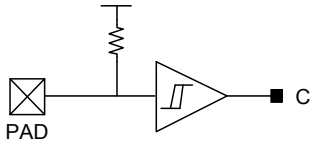
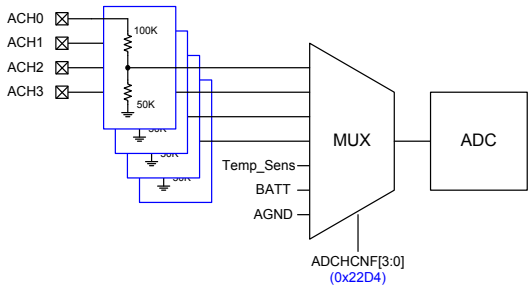
| Radio, Synthesizer, and Oscillator | | | |
|---|---|---|---|
| **Name** | **Pin** | **Type** | **Description** |
| AVDD3V1 | 16 | Power | 2.0V to 3.6V RF/Analog power supply connection |
| AVDD3V2 | 7 | Power | 2.0V to 3.6V RF/Analog power supply connection |
| ADCOUPL1 | 12 | Power | 1.8V RF/Analog power supply decoupling. Do not use for supplying external circuits. |
| ADCOUPL2 | 6 | Power | 1.8V RF/Analog power supply decoupling. Do not use for supplying external circuits. |
| ADCOUPL3 | 2 | Power | 1.8V RF/Analog power supply decoupling. Do not use for supplying external circuits. |
| AVDD18V | 48 | Power | 1.8V RF/Analog power supply connection |
| RF_P | 4 | RF I/O | Positive RF input signal to LNA in RX mode<br>Positive RF output signal from PA in TX mode |

| | | | |
|---|---|---|---|
| | | | It should be biased by ADCOUPL3. Refer to [Figure 3] in Sec.6. |
| RF_N | 3 | RF I/O | Negative RF input signal to LNA in RX mode<br>Negative RF output signal from PA in TX mode<br>It should be biased by ADCOUPL3. Refer to [Figure 3] in Sec.6. |
| RBIAS | 5 | Analog I/O | External precision bias resistor(510kohm) to generate the reference current |
| ACH0 | 8 | Analog I/O | ADC input |
| ACH1 | 9 | Analog I/O | ADC input |
| ACH2 | 10 | Analog I/O | ADC input |
| ACH3 | 11 | Analog I/O | ADC input |
| **Digital and Oscillator** | | | |
| **Name** | **Pin** | **Type** | **Description** |
| DVDD3V1 | 18 | Power | 2.0V to 3.6V Digital power supply connection |
| DVDD3V2 | 25,34 | Power | 2.0V to 3.6V Digital power supply connection |
| DVDD1 | 19 | Power | 1.8V Digital power supply decoupling.<br>*Note: Do not use for supplying external circuits.<br>*Note: It should not be connected together with DVDD2 (pin 44). |
| DVDD2 | 44 | Power | 1.8V Digital power supply decoupling.<br>*Note: Do not use for supplying external circuits.<br>*Note: It should not be connected together with DVDD1 (pin 19). |
| DXOSC18V | 47 | Power | 1.8V Digital power supply connection |
| RESETB | 17 | Digital input | Reset, active low |
| MS[0] | 13 | Digital input | Mode Selection<br>Value / Mode Configuration<br>000 / Normal mode with internal digital regulator<br>100 / ISP mode with internal digital regulator<br>others / Reserved |
| MS[1] | 14 | Digital input | |
| MS[2] | 15 | Digital input | |
| P0[0] | 43 | Digital I/O | Port P0.0/I2SRX_DI/PWM0, 16mA drive capability |
| P0[1] | 42 | Digital I/O | Port P0.1/I2SRX_LRCLK/PWM1, 16mA drive capability |
| P0[2] | 41 | Digital I/O | Port P0.2/I2SRX_BCLK/PWM2, 16mA drive capability |
| P0[3] | 40 | Digital I/O | Port P0.3/I2SRX_MCLK/PWM3, 16mA drive capability |
| P0[4] | 39 | Digital I/O | Port P0.4/I2STX_DO/PWM4, 16mA drive capability |
| P0[5] | 38 | Digital I/O | Port P0.5/I2STX_LRCLK/PTC_GATE0 |
| P0[6] | 37 | Digital I/O | Port P0.6/I2STX_BCLK/PTC_GATE1 |
| P0[7] | 36 | Digital I/O | Port P0.7/I2STX_MCLK/PTC_GATE2 |
| P1[0] | 26 | Digital I/O | Port P1.0/RXD1 |
| P1[1] | 24 | Digital I/O | Port P1.1/TXD1 |
| P1[3] | 23 | Digital I/O | Port P1.3/QUADZA/PTC_GATE3/IR_TX/CLK_OUT /XOSC32K_OUT |
| P1[4] | 22 | Digital I/O | Port P1.4/QUADZB/EXT_RTC_CLK/PTC_GATE4 /XOSC32K_IN |
| P1[6] | 21 | Digital I/O | Port P1.6/I2C_SCL/TRSWB |
| P1[7] | 20 | Digital I/O | Port P1.7/I2C_SDA/TRSW |

| | | | |
|---|---|---|---|
| P3[0] | 35 | Digital I/O | Port P3.0/RXD0/QUADXA |
| P3[1] | 33 | Digital I/O | Port P3.1/TXD0/QUADXB |
| P3[2] | 32 | Digital I/O | Port P3.2/nINT0 |
| P3[3] | 31 | Digital I/O | Port P3.3/nINT1 |
| P3[4] | 30 | Digital I/O | Port P3.4/RTS0/QUADYA/SPIDI/T0 |
| P3[5] | 29 | Digital I/O | Port P3.5/CTS0/QUADYB/SPIDO/T1 |
| P3[6] | 28 | Digital I/O | Port P3.6/RTS1/SPICLK |
| P3[7] | 27 | Digital I/O | Port P3.7/CTS1/SPICSN |
| XOSCI | 46 | Analog I/O | 32MHz crystal oscillator pin |
| XOSCO | 45 | Analog I/O | 32MHz crystal oscillator pin or external clock input |
| NC | 1 | | Do not connect. |
| **Ground** | | | |
| Exposed bottom | | Ground | Ground for RF, Analog, digital core, and I/O |

**Table 2. I/O Pins Equivalent Circuit Summary**

| Equivalent Circuit Schematic | Reset Status | Note |
|---|---|---|
| GPIO (P0[7:0], P1[1:0], P1[7:6], P3[7:0]) | | |
|  | Input with pull-up | I/O with the programmable pull-up/pull-down function |
| GPIO with 32.768kHz crystal oscillator buffer (P1[4:3]) | | |
|  | input with pull-up, crystal buffer disabled | Refer to Sec.8.18 (32.768kHz Crystal Oscillator). |
| MS[2],MS[1],MS[0] | | |

| | | |
|---|---|---|
|  | Input | |
| RESETB | | |
|  | Input | |
| ACH0, ACH1, ACH2, ACH3 | | |
|  | Analog Input | |

# 5. ELECTRICAL CHARACTERISTICS

## 5.1. Absolute Maximum Ratings

| Parameter | | Min. | Max | Unit | |
|---|---|---|---|---|---|
| Supply voltage(AVDD3V1,AVDD3V2, DVDD3V1,DVDD3V2) | | -0.3 | 3.6 | V | The voltage of all supply pins must be same. |
| Core voltage(ADCOUPL1,ADCOUPL2,ADCOUPL3,AVDD18V,DVDD1,DVDD2,DXOSC18V) | | -0.3 | 2 | V | |
| Storage Temperature | | -40 | 150 | °C | |
| ESD | HBM | | 2 | kV | All pads, according to human-body model(JEDEC STD 22) |
| | CDM | | 500 | V | According to charged-device model(JEDEC STD 22) |

Exceeding one or more of these ratings may cause permanent damage to the device.
These are stress ratings only, and the functional operation of the device at these or any other conditions beyond those indicated under “ELECTRICAL SPECIFICATIONS” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**NOTE**: These values were obtained under worst-case test conditions specially prepared for the MG2471 and these conditions are not sustained in normal operation environment.

**CAUTION**: *ESD sensitive device. Precaution should be used when handling the device to prevent permanent damage.*

## 5.2. Recommended Operating Conditions

| Parameter | MIN | MAX | UNIT |
|---|---|---|---|
| Operating ambient temperature range, $T_{OP}$ | -40 | 85 | ℃ |
| Operating supply voltage, VDD (AVDD3V1,AVDD3V2,DVDD3V1,DVDD3V2) | 2 | 3.6 | V |
| Voltage on any digital pin | -0.3 | VDD | V |

## 5.3. DC Characteristics

All voltage values are based on Ground.

| Parameter | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| VDD Operating Supply Voltage | | | | | |
| | VDD=3.30V | 3.00 | | 3.60 | V |
| | VDD=3.00V | 2.70 | | 3.30 | |
| | VDD=2.56V | 2.30 | | 2.82 | |
| | VDD=2.20V | 2.00 | | 2.42 | |

| | | | | | |
|---|---|---|---|---|---|
| $V_{IH}$ | Logic-high Input Voltage | | | | |
| | VDD=3.30V | 2.10 | | 3.60 | V |
| | VDD=3.00V | 1.90 | | 3.30 | |
| | VDD=2.56V | 1.70 | | 2.82 | |
| | VDD=2.20V | 1.50 | | 2.42 | |
| $V_{IL}$ | Logic-low Input Voltage | | | | |
| | VDD=3.30V | -0.3 | | 0.8 | V |
| | VDD=3.00V | -0.3 | | 0.7 | |
| | VDD=2.56V | -0.3 | | 0.6 | |
| | VDD=2.20V | -0.3 | | 0.5 | |
| $R_{PU}$ | Pull-up Resistor | | | | |
| | VDD=3.30V | 34K | 48K | 72K | Ω |
| | VDD=3.00V | 37K | 54K | 82K | |
| | VDD=2.56V | 44K | 66K | 101K | |
| | VDD=2.20V | 53K | 81K | 125K | |
| $R_{PD}$ | Pull-down Resistor | | | | |
| | VDD=3.30V | 28K | 47K | 90K | Ω |
| | VDD=3.00V | 30K | 51K | 102K | |
| | VDD=2.56V | 33K | 62K | 128K | |
| | VDD=2.20V | 39K | 76K | 161K | |
| $V_{OL}$ | Output Low Voltage | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | VDD*0.73 | | | V |
| $I_{OL}$ | Low-level Output Current @$V_{OL}$(max)[1] | | | | |
| | VDD=3.30V (DS=0) | 6.3 | | | mA |
| | VDD=3.00V (DS=0) | 5.7 | | | |
| | VDD=2.56V (DS=0) | 4.8 | | | |
| | VDD=2.20V (DS=0) | 3.9 | | | |
| | VDD=3.30V (DS=1) | 9.5 | | | |
| | VDD=3.00V (DS=1) | 8.6 | | | |
| | VDD=2.56V (DS=1) | 7.2 | | | |
| | VDD=2.20V (DS=1) | 5.9 | | | |
| $I_{OH}$ | High-level Output Current @$V_{OH}$(min)[2] | | | | |
| | VDD=3.30V (DS=0) | 7.4 | | | mA |
| | VDD=3.00V (DS=0) | 5.9 | | | |
| | VDD=2.56V (DS=0) | 4.3 | | | |
| | VDD=2.20V (DS=0) | 3.3 | | | |
| | VDD=3.30V (DS=1) | 11.2 | | | |
| | VDD=3.00V (DS=1) | 8.9 | | | |
| | VDD=2.56V (DS=1) | 6.5 | | | |
| | VDD=2.20V (DS=1) | 5.0 | | | |

[1] For P0[7:5], P1[1:0], P1[4:3], P1[7:6], and P3[7:0] pins
[2] For P0[7:5], P1[1:0], P1[4:3], P1[7:6], and P3[7:0] pins

## 5.4. Current Consumption and Timing Characteristics

$T_{OP}$ = 25˚C, VDD=3.0V, unless otherwise noted.

| Parameter(Condition) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| MCU active. No radio and peripherals (UART1&RNG) active.<br>@ MCU clock = 8MHz<br>@ MCU clock = 16MHz | | <br>4.2<br>5.2 | | mA |
| RX mode. MCU active @ MCU clock = 8MHz | | 24.9 | | mA |
| TX mode. MCU active @ MCU clock = 8MHz<br>@ maximum transmit output power<br>@ 0dBm | | <br>36.5<br>22.5 | | mA |
| Power mode1.<br>Digital regulator on, 16MHz RCOSC and 32MHz crystal oscillator off, 32kHz RCOSC, POR, BOD, and sleep timer active. | | 35.3 | 44.4 | µA |
| Power mode1.<br>Digital regulator on, 16MHz RCOSC, 32MHz crystal oscillator off, 32.768kHz crystal oscillator, POR, BOD, and sleep timer active. | | 45.3 | 54.4 | µA |
| Power mode2.<br>Digital regulator off, 16MHz RCOSC, 32MHz crystal oscillator off, 32kHz RCOSC and sleep timer active. | | 1.8 | 4.1 | µA |
| Power mode2.<br>Digital regulator off, 16MHz RCOSC, 32MHz crystal oscillator off, 32.768kHz crystal oscillator and sleep timer active. | | 11.8 | 14.1 | µA |
| Power mode3.<br>Digital regulator off, 16MHz RCOSC, 32MHz crystal oscillator off, 32kHz RCOSC(32.768kHz crystal oscillator) and sleep timer off. | | | 1 | µA |
| **Wake-up and timing** | | | | |
| Power mode1 → MCU Active<br>Digital regulator on, 16MHz RCOSC and 32MHz crystal oscillator off. Start-up of 16MHz RCOSC | | 5 | | µs |
| Power mode2 → MCU Active<br>Digital regulator off, 16MHz RCOSC and 32MHz crystal oscillator off. Start-up of regulator and 16MHz RCOSC | | 100 | | µs |
| MCU Active → TX or RX<br>Initially running on 16MHz RCOSC, Added start-up time of 32MHz crystal oscillator. | | 992 | | µs |
| TX/RX and RX/TX turnaround | | | 192 | µs |

## 5.5. RF Receive Section

Measured on 2-layer reference design with $T_{OP}$=25℃, VDD=3.0V, and fc=2450MHz, unless otherwise noted.

| Parameter(Condition) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| RF frequency range[3](center frequency) | 2405 | | 2480 | MHz |
| Maximum input level (PER=1%)<br>@ 1000kbps<br>@ 500kbps<br>@ 250kbps<br>@ 125kbps<br>@ 62.5kbps<br>@ 31.25kbps | | <br>-6<br>-9<br>-2<br>-4<br>5<br>5 | | dBm |
| Spurious radiation<br>@ 30MHz – 1000MHz | | <br>-73.7 | | dBm |

[3] Extended range: 2394~2507MHz

| | | | | |
|---|---|---|---|---|
| @ 1GHz – 12.75GHz | | -73.7 | | |
| Received RF bandwidth | | 2 | | MHz |
| Channel spacing[4] | | 5 | | MHz |
| Receiver sensitivity (PER≤1%, PSDU length of 20-byte)<br>@ 1000kbps<br>@ 500kbps<br>@ 250kbps<br>@ 125kbps<br>@ 62.5kbps<br>@ 31.25kbps | | <br>-93<br>-91<br>-98<br>-99<br>-103<br>-105 | | dBm |
| Adjacent channel rejection (Sensitivity+3, adjacent modulated channel at ±5MHz, PER=1%, 250kbps)<br>+5MHz<br>-5MHz | | <br>27<br>27 | | dB |
| Alternate channel rejection (Sensitivity+3, adjacent modulated channel at ±10MHz, PER=1%, 250kbps)<br>+10MHz<br>-10MHz | | <br>48<br>47 | | dB |
| Others channel rejection (Sensitivity+3, adjacent modulated channel at over ±15MHz, PER=1%, 250kbps)<br>≥+15MHz<br>≥-15MHz | | <br>53<br>52 | | dB |
| Co-channel rejection (Sensitivity+3. Undesired IEEE 802.15.4 modulated signal at the same frequency. Signal level for PER=1%, 250kbps) | | -8.9 | | dB |
| Blocking/desensitization<br>-250MHz<br>-100MHz<br>-50MHz<br>+50MHz<br>+100MHz<br>+250MHz | | <br>-25<br>-35<br>-38<br>-37<br>-35<br>-31 | | dBm |
| RSSI dynamic range | | | 80 | dB |
| RSSI accuracy | | ± 3 | | dB |

## 5.6. RF Transmit Section

Measured on 2-layer reference design with $T_{OP}$=25℃, VDD=3.0V, and fc=2450MHz, unless otherwise noted.

| Parameter(Condition) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| RF frequency range[5](center frequency) | 2405 | | 2480 | MHz |
| TX output power (using the recommended matching circuit) | | +9.0 | | dBm |
| Transmit chip rate | | 2 | | Mcps |
| Error vector magnitude (EVM) | | 7 | | % |
| Harmonics<br>2nd harmonic<br>3rd harmonic | | <br>-43.9<br>-51.0 | | dBm |
| Spurious emission (complies with EN 300-440, FCC and ARIB STD-T66)<br>30Hz ~ 1GHz<br>1GHz ~ 12.75GHz | | <br>< -75<br>< -43.9 | | dBm |

[4] Specified in IEEE Standard 802.15.4™
[5] Extended range: 2394~2507MHz

| | | | | |
|---|---|---|---|---|
| 1.8 ~ 1.9GHz<br>5.15 ~ 5.3GHz | | < -75<br>< -75 | | |

## 5.7. Frequency Synthesizer

$T_{OP}$=25℃, VDD=3.0V, and fc=2450MHz, unless otherwise noted.

| Parameter(Condition) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Phase noise, unmodulated carrier<br>@ ±100kHz offset<br>@ ±1MHz offset<br>@ ±2MHz offset<br>@ ±3MHz offset<br>@ ±5MHz offset<br>@ ±10MHz offset<br>@ ±50MHz offset | | <br>-76.5<br>-99.6<br>-108.6<br>-112.7<br>-115.2<br>-121.2<br>-140.9 | | dBc/Hz |
| Lock time | | 97 | | μs |

## 5.8. 32MHz Crystal Oscillator

$T_{OP}$=25℃, DXOSC18V=1.8V, unless otherwise noted.

| Parameter(Condition) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Crystal frequency | | 32 | | MHz |
| Crystal frequency accuracy requirement | -40 | | 40 | ppm |
| Equivalent series resistance(ESR) | | 30[6] | 60[7] | Ω |
| Crystal shunt capacitance($C_O$) | | 3 | 5 | pF |
| Crystal load capacitance($C_L$) | | 13[6] | 16[7] | pF |
| Start-up time | | | 0.8 | ms |

## 5.9. 16MHz RC Oscillator

$T_{OP}$=25℃, DXOSC18V=1.8V, unless otherwise noted.

| Parameter(Condition) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Frequency | | 16 | | MHz |
| Frequency accuracy before calibration | -25 | | 25 | % |
| Frequency accuracy after calibration | -3 | | 3 | % |
| Initial calibration time | | 50 | | μs |
| Start-up time | | | 1 | μs |

[6] The negative resistance of driving circuit is five times larger than the ESR of crystal oscillator with crystal satisfying above TYP conditions.
[7] The negative resistance of driving circuit is two times larger than the ESR of crystal oscillator with crystal satisfying above MAX conditions.

## 5.10. 32kHz RC Oscillator

$T_{OP}$=25℃, VDD=3.0V, unless otherwise noted.

| Parameter(Condition) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Calibrated frequency | | 32.787 | | kHz |
| frequency accuracy after calibration | -0.3 | | 0.3 | % |
| Initial calibration time | | 1 | | ms |
| Start-up time | | | 100 | μs |

## 5.11. 32.768kHz Crystal Oscillator

$T_{OP}$=25℃, VDD=3.0V, unless otherwise noted.

| Parameter(Condition) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Frequency | | 32.768 | | kHz |
| Crystal frequency accuracy requirement | -40 | | 40 | ppm |
| Equivalent series resistance(ESR) | | 50 | 100 | kΩ |
| Crystal shunt capacitance($C_O$) | | 0.9 | | pF |
| Crystal load capacitance($C_L$) | | 12.5 | | pF |
| Start-up time | | 1.2 | | s |

## 5.12. Temperature Sensor

VDD=3.0V, unless otherwise noted.

| Parameter(Condition) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Output at -40℃ | | -295 | | |
| Output at 25℃ | | 76 | | |
| Output at 85℃ | | 418 | | |
| Temperature coefficient | | 5.703 | | /℃ |

All measurement results are obtained using the 12-bit ADC.

## 5.13. ADC

$T_{OP}$=25℃, VDD=3.0V, unless otherwise noted.

| Parameter(Condition) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | 0 | | VDD | V |
| Input resistance | | 150 | | kΩ |
| Full-scale signal | | | 3 | V |
| Effective number of bits(ENOB)<br>Single-ended input, 12bit setting | | 10.8 | | bits |
| Signal to noise and distortion(SINAD)<br>Single-ended input, 12bit setting | | 66.78 | | dB |
| Current consumption | | 0.46 | | mA |
| Internal reference voltage | | 1.25 | | V |

## 5.14. Flash Memory

### 5.14.1. Flash memory characteristics

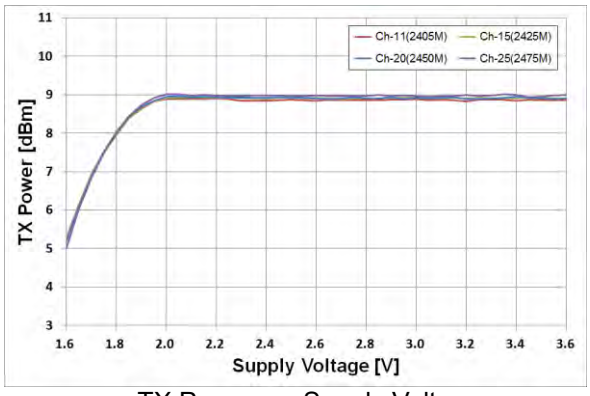
| Characteristic | Symbol | Conditions | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Endurance | Nendu | 20ms erase and 20 us program time at 1.8V | 20,000 | | | cycles |
| Data retention | Tret | 25 °C | 100 | | | years |

### 5.14.2. Flash memory and page size

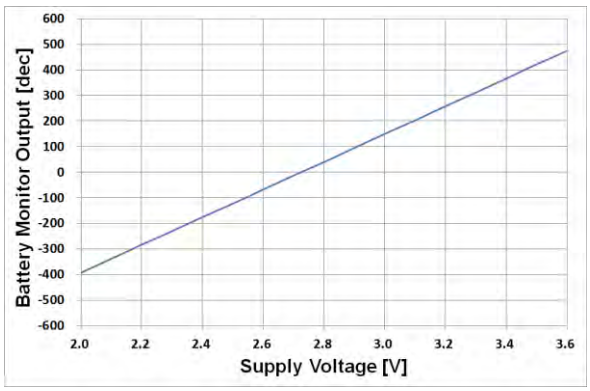
| Name | Size | Unit |
|---|---|---|
| Flash main memory block | 65,536 | bytes |
| Flash information block | 1,024 | bytes |
| Flash page size | 512 | bytes |

## 5.15. Typical Performance Curves

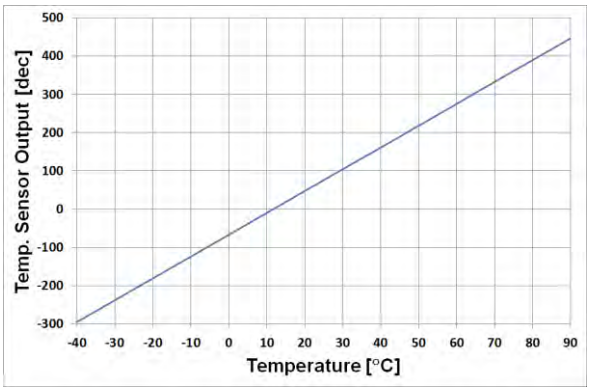
$T_{OP}$=25℃, VDD=3.0V, and fc=2450MHz, unless otherwise noted. All parameters measured on 2-layer reference design.




TX Power vs. Supply Voltage




ADC – Battery monitoring output




ADC – Temperature sensor output

# 6. REFERENCE APPLICATION CIRCUITS

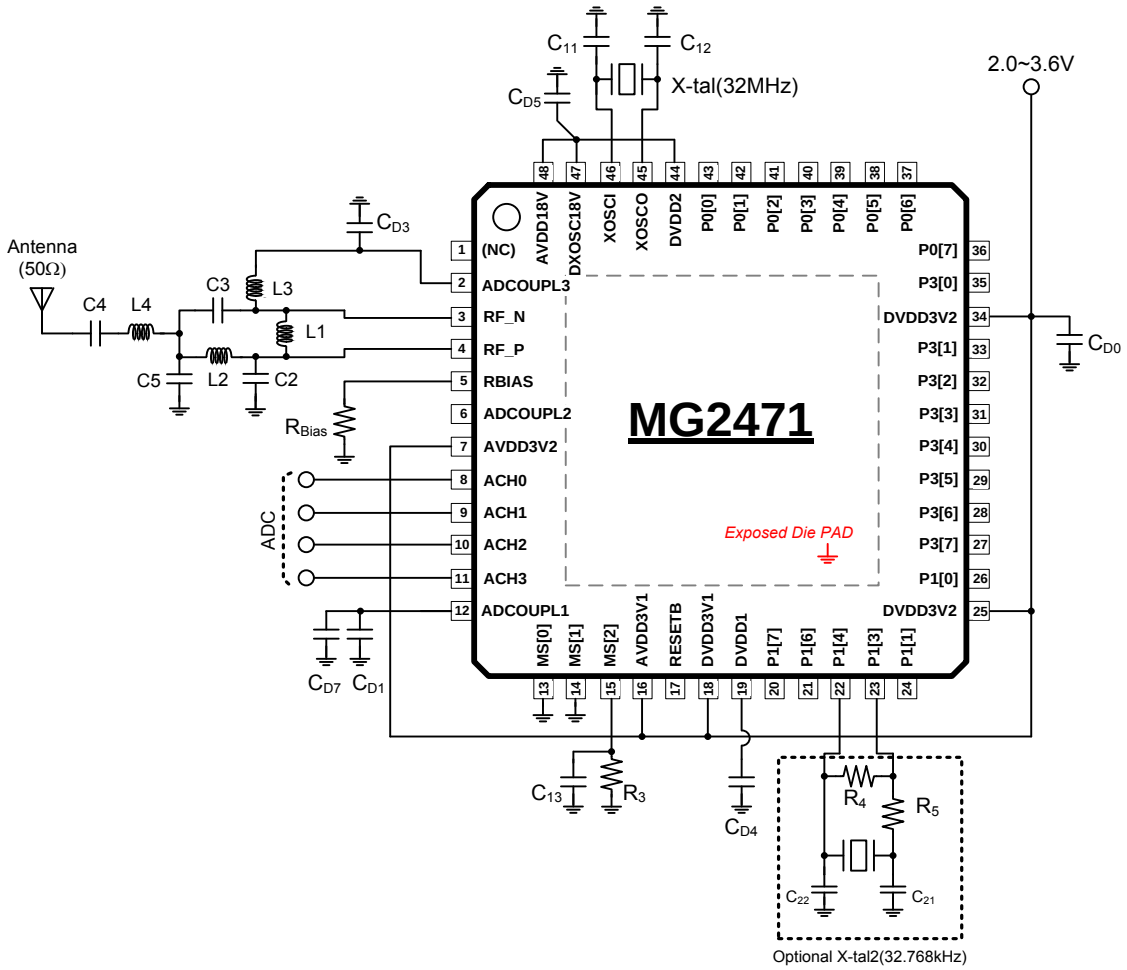
A typical application diagram of the MG2471 is shown in [Figure 3]. Only a few external components are required for the operation of the MG2471. [Table 3] describes the external components including decoupling capacitors.

The inductor, L1 is used as a matching component for the LNA and as an output load for the PA, respectively. The components near the RF_P/RF_N pins, L2, L3, C2, and C3 form a balun which converts the differential RF signals to a single-ended RF signal. And, L4, C4, and C5 form a LC harmonic filter to suppress the TX output harmonics. In addition, C4 is needed for DC blocking. All together with adequate values, they also transform the impedance to match a 50-Ohm antenna.

As shown in [Figure 3], RF_P and RF_N are biased by ADCOUPL3 through L1 and L3.

The 32MHz crystal provides the reference frequency source for MG2471. C11 and C12 are loading capacitors of it. $C_{D0}$, $C_{D1}$, $C_{D3}$, $C_{D4}$, $C_{D5}$, $C_{D7}$, and $C_7$ are supply decoupling capacitors, whose values depend on PCB artwork and stack-up information.

The components' values listed in Table 3 are selected for 2-layer reference PCB design.




**** GND is bottom pad (down-bonding pad) in the above schematic*

**Figure 3. MG2471 Typical Application Circuit**

In applications, some GPIO pins (among P0, P1 and P3) and ADC input pins may be unused. Then, the unused GPIO pins are recommended to be floating and configured as the input pull-up state: the input pull-up is the default state of the GPIOs. For the detail register configuration on the GPIOs, please refer to the Sec 8.2. Similarly, the unused ADC input pins are recommended to be connected to the ground.

**Table 3. Bill of Materials for Figure 3**

| No | Component | Description | Value |
|---|---|---|---|
| 1 | L1 | RF matching inductor | 2.4nH |
| 2 | L2, L3 | RF balun inductors | 4.7nH |
| 3 | C2, C3 | RF balun capacitors | 0.75pF |
| 4 | L4 | RF LC filter/matching inductor | 5.1nH |
| 5 | C5 | RF LC filter/matching capacitor | 0.5pF |
| 6 | C4 | RF matching/DC blocking capacitor | 1.0pF |
| 7 | Rbias | Resistor for internal bias current reference | 510kohm |
| 8 | X-tal | 32MHz crystal unit | 32MHz |
| 9 | C11, C12 | Crystal loading capacitors | 13pF[8] |
| 10 | $C_{D0}$ | Decoupling capacitor for DVDD3V | 10uF |
| 11 | $C_{D1}$ | Decoupling capacitor for ADCOUPL1 | 1uF |
| 12 | $C_{D7}$ | Decoupling capacitor for ADCOUPL1 | 1uF |
| 13 | $C_{D3}$ | Decoupling capacitor for ADCOUPL3 | 1uF |
| 14 | $C_{D4}$ | Decoupling capacitor for DVDD1 | 1uF |
| 15 | $C_{D5}$ | Decoupling capacitor for DVDD2 and DXOSC18V | 100pF |
| 16 | $R_3$ | Pull-down resistor for MS[2] input | 10kohm |
| 18 | $C_{13}$ | Capacitor for MS[2] input | 1uF |
| 19 | $C_{21}$ | (option) Capacitor for 32.768kHz crystal oscillator | 33pF |
| 20 | $C_{22}$ | (option) Capacitor for 32.768kHz crystal oscillator | 15pF |
| 21 | $R_4$ | (option) Resistor for 32.768kHz crystal oscillator | 22Mohm |
| 22 | $R_5$ | (option) Resistor for 32.768kHz crystal oscillator | 330kohm |

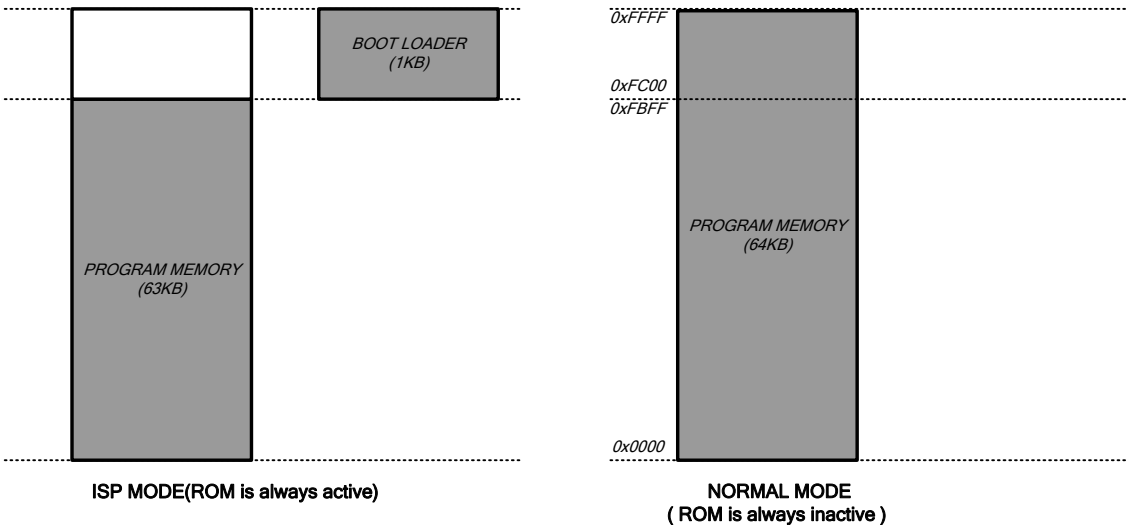
[8] The value of crystal loading capacitance depends on crystal oscillator.

# 7. MCU SUBSYSTEM

## 7.1. Memory Organization

### 7.1.1. Program Memory

The address space of program memory is 64KB (0x0000~0xFFFF). Basically, the lower 63KB of program memory is implemented by non-volatile memory. The upper 1KB from 0xFC00 to 0xFFFF is implemented by both non-volatile memory and ROM. As shown in [Figure 4] below, there are two types of memory in the same address space. The address space, which is implemented by non-volatile memory, is used as general program memory and the address space, which is implemented by ROM, is used for ISP (In-System Programming).
As shown in (a) of [Figure 4] below, when Power is turned on, the upper 1KB of program memory is mapped to ROM under the ISP mode. As shown in (b) of [Figure 4], this program area (1KB) is used as non-volatile program memory under the normal mode. The ROM area can't be accessed under the normal mode.




(a) (b)

**Figure 4. Address Map of Program Memory**

### 7.1.2. Data Memory

MG2471 reserves 64 KB data memory address space. This address space can be accessed by MOVX instruction. [Figure 5] shows the address map of MG2471 data memory.

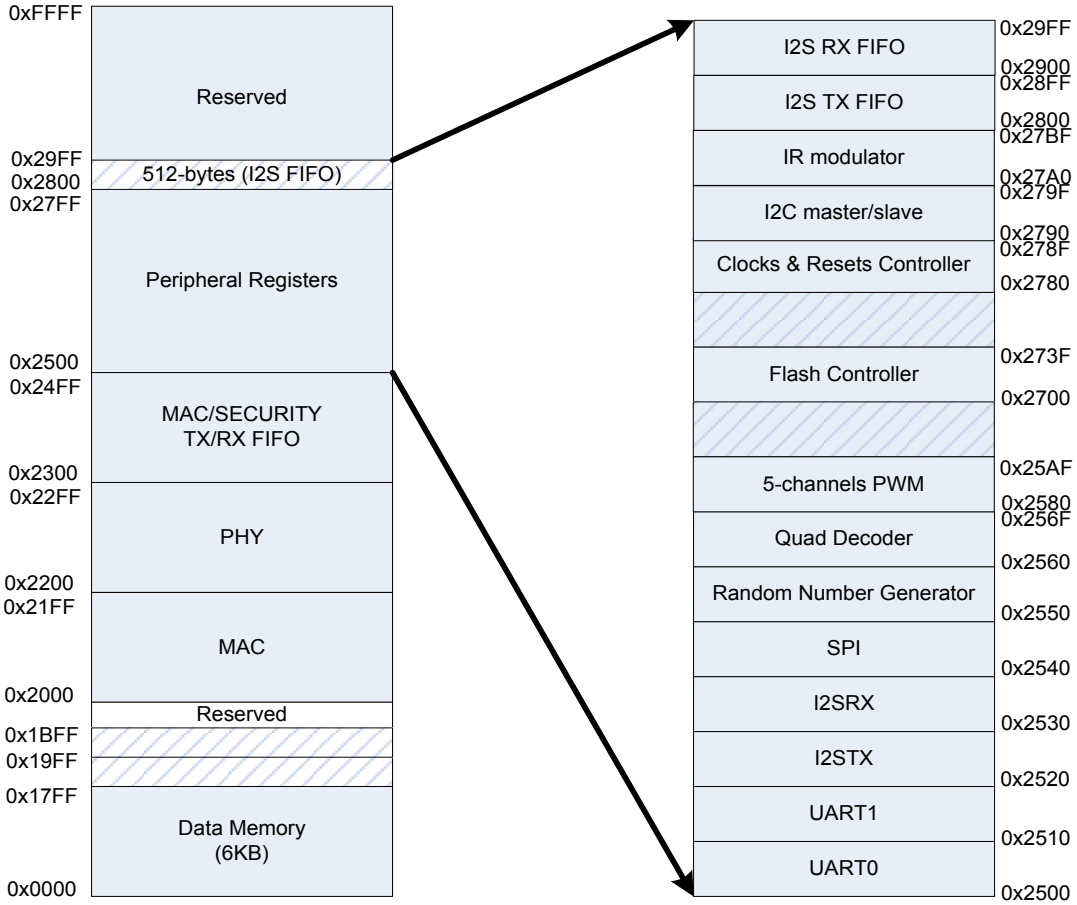



**Figure 5. Address Map of Data Memory**

The data memory used in the application programs resides in the address range 0x0000-0x17FF. The registers and memory used in the MAC block reside in the address range 0x2000-0x21FF and 0x2300-0x24FF respectively. The registers to control or report the status of PHY block reside in the address range 0x2200-0x22FF.
Registers related to the numerous peripheral functions of the embedded microprocessor reside in the address range of 0x2500-0x29FF.

### 7.1.3. General Purpose Registers

[Figure 6] describes the address map of the General Purpose Registers (GPRs). GPRs can be addressed either directly or indirectly. As shown in the lower address space of [Figure 6], a bank consists of 8 registers.
The address space above the bank area is the bit addressable area, which is used as a flag by software or by a bit operation. The address space above the bit addressable area includes registers used as a general purpose of a byte unit. For more detailed information, refer to the paragraphs following [Figure 6] below.

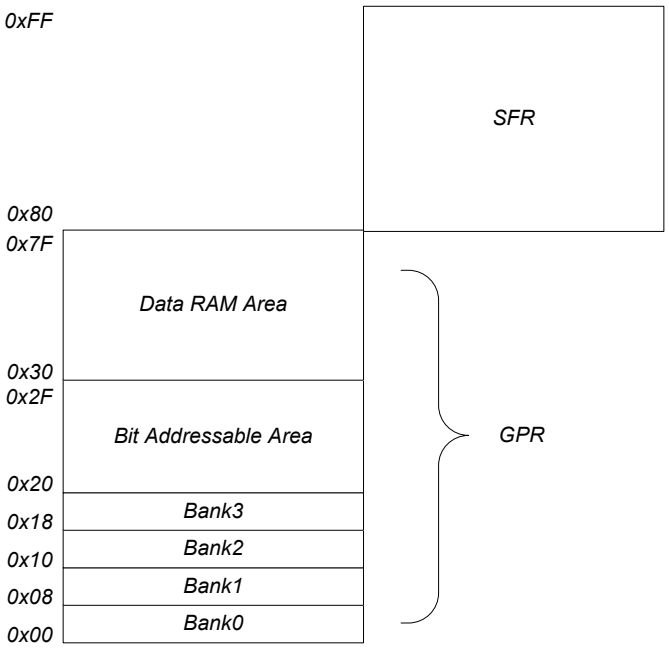



**Figure 6. GPRs Address Map**

**Register Bank 0-3:** It is located from 0x00 to 0x1F (32 bytes). One bank consists of each 8 registers out of 32 registers. Therefore, there are total 4 banks. Each bank should be selected by software as referring the RS field in PSW register. The bank (8 registers) selected by RS value can be accessed by a name (R0-R7) by software. After reset, the default value is set to bank0.

**Bit Addressable Area:** The address is assigned to each bit of 16 bytes (0x20~0x2F) and registers, which is the multiple of 8, in SFR. Each bit can be accessed by the address which is assigned to these bits. 128 bits (16 bytes, 0x20~0x2F) can be accessed by direct addressing for each bit (0x00~0x7F address is assigned) and by a byte unit as using the address from 0x20~0x2F.

Data RAM Area: A user can use the data memory area (0x30~0x7F) as a general purpose.

### 7.1.4. Special Function Registers(SFR)

The special function registers (SFRs) reside in their associated peripherals or in the 8051 core.
The SFR include the status or control register of the I/O ports, the timer registers, the stack pointers and so on. [Table 4] shows the address to all SFRs in MG2471. Unoccupied locations in the SFR space (the blank locations in Table 4) are unimplemented, i.e., no register exists.
If an instruction attempts to write to an unimplemented SFR location, the instruction executes, but nothing is actually written. If an unimplemented SFR location is read, it returns a zero value.
All SFRs are accessed by a byte unit. However, when SFR address is multiple of 8, it can be accessed by a bit unit.

**Table 4. SFR (Special Function Register) Memory Map**

| SFR Address | 8 bytes | | | | | | | | SFR Address |
|---|---|---|---|---|---|---|---|---|---|
| **80** | P0 | SP | DPL | DPH | | | | PCON | **87** |
| **88** | TCON | TMOD | TL0 | TL1 | TH0 | TH1 | CLKCON1 | CLKCON2 | **8F** |
| **90** | P1 | EXIF1 | PERI_CLK_STP3 | | | | | | **97** |
| **98** | PERI_CLK_STP0 | PERI_CLK_STP1 | PERI_CLK_STP2 | | P1SRC_SEL | | | | **9F** |
| **A0** | | | AUXR1 | | | | | | **A7** |
| **A8** | IE | T23CON | TH2 | TH3 | TL2 | TL3 | | | **AF** |
| **B0** | P3 | P0OEN | P1OEN | | P3OEN | | | | **B7** |
| **B8** | IP | P0_IE | P1_IE | | P3_IE | | | | **BF** |
| **C0** | WCON | P0_DS | P1_DS | | P3_DS | | | | **C7** |
| **C8** | | | | | | | | | **CF** |
| **D0** | PSW | | WDTCON | | | | | | **D7** |
| **D8** | EXIF2 | | | | | | | | **DF** |
| **E0** | ACC | | | | | | | | **E7** |
| **E8** | EIE1 | EIE2 | P0_POL | P0_EDGE | P0_IRQ_EN | P0_IRQ_STS | | | **EF** |
| **F0** | B | GPIO_IRQ_PEND | P1_POL | P1_EDGE | P1_IRQ_EN | P1_IRQ_STS | | | **F7** |
| **F8** | EIP2 | EIP2 | P3_POL | P3_EDGE | P3_IRQ_EN | P3_IRQ_STS | | | **FF** |

The following section describes each SFR relating to microprocessor.

***Note 1: This table shows register bit symbol conventions.***

| Symbol | Access Mode |
|---|---|
| RW | Read/Write |
| RO | Read Only |
| WO | Write Only |

**WCON (WRITE CONTROL REGISTER, 0xC0)**

This register can control the upper 1KB of program memory.

| Bit | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:5 | | Reserved | RO | 0 |
| 4 | ISPMODE | ISP Mode Indication.<br>When MS[2:0], an external pin, is ‘100’, this field is set to 1 by hardware. It notifies the MCU whether ISPMODE or not. | RO | - |
| 3 | | Reserved | RO | 0 |
| 2 | | Reserved | RO | 0 |
| 1 | ENROM | When this field is ‘1’, the upper 1KB (0xFC00~0xFFFF) is mapped to ROM. When this field is ‘0’, the upper 1KB (0xFC00~0xFFFF) is mapped to non-volatile memory. The bit setting is effective under the ISP mode. | R/W | 1 |

| | | | | |
|---|---|---|---|---|
| 0 | | Reserved | | 0 |

**ACCUMULATOR (A or ACC, 0xE0)**
This register is marked as A or ACC and it is related to all the operations.

| Bit | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | A | Accumulator | R/W | 0x00 |

**B REGISTER (B, 0xF0)**
This register is used for a special purpose when multiplication and division are processed. For other instructions, it can be used as a general-purpose register. After multiplication is processed, this register contains the MSB data and 'A register' contains LSB data for the multiplication result. In division operation, this register stores the value before division (dividend) and the remainder after division. At this time, before division, the divisor should be stored in 'A register' and result value (quotient) is stored in it after division.

| Bit | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | B | B register. Used in MUL/DIV instructions. | R/W | 0x00 |

**PROGRAM STATUS WORD (PSW, 0xD0)**
This register stores the status of the program. The explanation of each bit is as follows.

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| 7 | CY | Carry flag | R/W | 0 |
| 6 | AC | Auxiliary carry flag | R/W | 0 |
| 5 | F0 | Flag0. User-defined | R/W | 0 |
| 4:3 | RS | Register bank select.<br>0: Bank0<br>1: Bank1<br>2: Bank2<br>3: Bank3 | R/W | 0 |
| 2 | OV | Overflow flag | R/W | 0 |
| 1 | F1 | Flag1. User-defined | R/W | 0 |
| 0 | P | Parity flag.<br>Set to 1 when the value in accumulator has odd number of '1' bits. | R/W | 0 |

**STACK POINTER (SP, 0x81)**
When PUSH and CALL instructions are executed, some data (like the parameters by function call) are stored in stack to inform the values. In embedded MCU, the data memory area which can be used for a general purpose (0x08~0x7F) is used as a stack area.
This register value is increased before the data is stored and decreased after the data is read when the POP and RET instructions are executed. The default value is 0x07.

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| 7:0 | SP | Stack Pointer | R/W | 0x07 |

**DATA POINTER (DPH : 0x83, DPL : 0x82)**
Data pointer consists of a high byte (DPH) and a low byte (DPL) to support 16-bit address. It can be accessed by 16-bit register or by two 8-bit registers respectively.

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| 7:0 | DPH | Data pointer, high byte | R/W | 0x00 |

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| 7:0 | DPL | Data pointer, low byte | R/W | 0x00 |

**AUXILIARY CONTROL REGISTER (AUXR1, 0xA2)**

This register is used to implement the Dual DPTR functions. Physically, The DPTR consists of DPTR0 and DPTR1. However, DPTR0 and DPTR1 can be accessed depending on the DPS value of AUXR1 respectively. In other words, they cannot be accessed at the same time.

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| 7:1 | | Reserved | RO | 0x00 |
| 0 | DPS | Dual DPTR Select: Used to select either DPTR0 or DPTR1.<br>When DPS is '0', DPTR0 is selected. When DPS is '1', DPTR1 is selected. | R/W | 0 |

**GPIO SFRs**

Please refer to Sec 8.2. GPIO for more details.

| Register | Address | Description |
|---|---|---|
| P0 | 0x80 | PORT-0 data register |
| P1 | 0x90 | PORT-1 data register |
| P1SRC_SEL | 0x9C | PORT-1 source control register |
| P3 | 0xB0 | PORT-3 data register |
| P0OEN | 0xB1 | PORT-0 direction register |
| P1OEN | 0xB2 | PORT-1 direction register |
| P3OEN | 0xB4 | PORT-3 direction register |
| P0_IE | 0xB9 | PORT-0 input enable register |
| P1_IE | 0xBA | PORT-1 input enable register |
| P3_IE | 0xBC | PORT-3 input enable register |
| P0_DS | 0xC1 | PORT-0 drive strength selection register |
| P1_DS | 0xC2 | PORT-1drive strength selection register |
| P3_DS | 0xC4 | PORT-3 drive strength selection register |
| P0_POL | 0xEA | P0[7:0] interrupt polarity selection register |
| P0_EDGE | 0xEB | P0[7:0] interrupt edge selection register |
| P0_IRQ_EN | 0xEC | P0[7:0] interrupt enable register |
| P0_IRQ_STS | 0xED | P0[7:0] interrupt flags register |
| P1_POL | 0xF2 | P1[7:0] interrupt polarity selection register |
| P1_EDGE | 0xF3 | P1[7:0] interrupt edge selection register |
| P1_IRQ_EN | 0xF4 | P1[7:0] interrupt enable register |
| P1_IRQ_STS | 0xF5 | P1[7:0] interrupt flags register |
| P3_POL | 0xFA | P3[7:0] interrupt polarity selection register |
| P3_EDGE | 0xFB | P3[7:0] interrupt edge selection register |
| P3_IRQ_EN | 0xFC | P3[7:0] interrupt enable register |
| P3_IRQ_STS | 0xFD | P3[7:0] interrupt flags register |

**WDT (WATCHDOG TIMER) SFR**

Please refer to Sec 8.6. WDT for the more details.

| Register | Address | Description |
|---|---|---|
| WDTCON | 0xD2 | Watchdog timer control register |

**Timer 0/1 SFRs**

Please refer to Sec 8.3. timer 0/1 for the more details.

| Register | Address | Description |
|---|---|---|
| TCON | 0x88 | Timer/Counter 0 & 1 control |
| TMOD | 0x89 | Timer/Counter 0 & 1 mode control |
| TL0 | 0x8A | Timer/Counter 0 low byte |
| TH0 | 0x8C | Timer/Counter 0 high byte |
| TL1 | 0x8B | Timer/Counter 1 low byte |
| TH1 | 0x8D | Timer/Counter 1 high byte |

**Timer 2/3 SFRs**

Please refer to Sec 8.4 timer 2/3 for the more details.

| Register | Address | Description |
|---|---|---|
| T23CON | 0xA9 | Timer 2 & 3 control |
| TL2 | 0xAC | Timer2 low byte |
| TH2 | 0xAA | Timer2 high byte |
| TL3 | 0xAD | Timer3 low byte |
| TH3 | 0xAB | Timer3 high byte |

**8051 MCU Clock Control SFRs**

Please refer to Sec 7.2. clock for the more details.

| Register | Address | Description |
|---|---|---|
| CLKCON1 | 0x8E | MCU subsystem reference clock control 1 |
| CLKCON2 | 0x8F | MCU subsystem reference clock control 2 |
| PERI_CLK_STP0 | 0x98 | MCU peripherals clock on/off control 0 |
| PERI_CLK_STP1 | 0x99 | MCU peripherals clock on/off control 1 |
| PERI_CLK_STP2 | 0x9A | MCU peripherals clock on/off control 2 |
| PERI_CLK_STP3 | 0x92 | MCU peripherals clock on/off control 3 |

**Power Control SFR**

Please refer to Sec 8.15. power management for the more details.

| Register | Address | Description |
|---|---|---|
| PCON | 0x87 | Power control register |

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| 7:2 | | Reserved bits | RO | 0 |
| 1 | PD | Power-down mode bit<br>1: start power-down mode<br>0: clear by hardware when an enabled external interrupt or a reset occurs. | R/W | 0 |
| 0 | | Reserved bit | RO | 0 |

**8051 MCU Interrupt SFRs**

Please refer to Sec 7.4. interrupts for the more details.

| Register | Address | Description |
|---|---|---|
| IE | 0xA8 | Interrupt Enable |
| EIE1 | 0xE8 | Extended Interrupt Enable 1 |

| | | |
|---|---|---|
| EIE2 | 0xE9 | Extended Interrupt Enable 2 |
| IP | 0xB8 | Interrupt Priority |
| EIP1 | 0xF8 | Extended Interrupt Priority 1 |
| EIP2 | 0xF9 | Extended Interrupt Priority 2 |
| EXIF2 | 0xD8 | Extended Interrupt Flag 2 |
| EXIF1 | 0x91 | Extended Interrupt Flag 1 |

## 7.2. Clock

The MG2471 supports an advanced and flexible clock selection function to reduce the power consumption depending on the target applications. The clock system overview of MG2471 is shown in the [Figure 7].

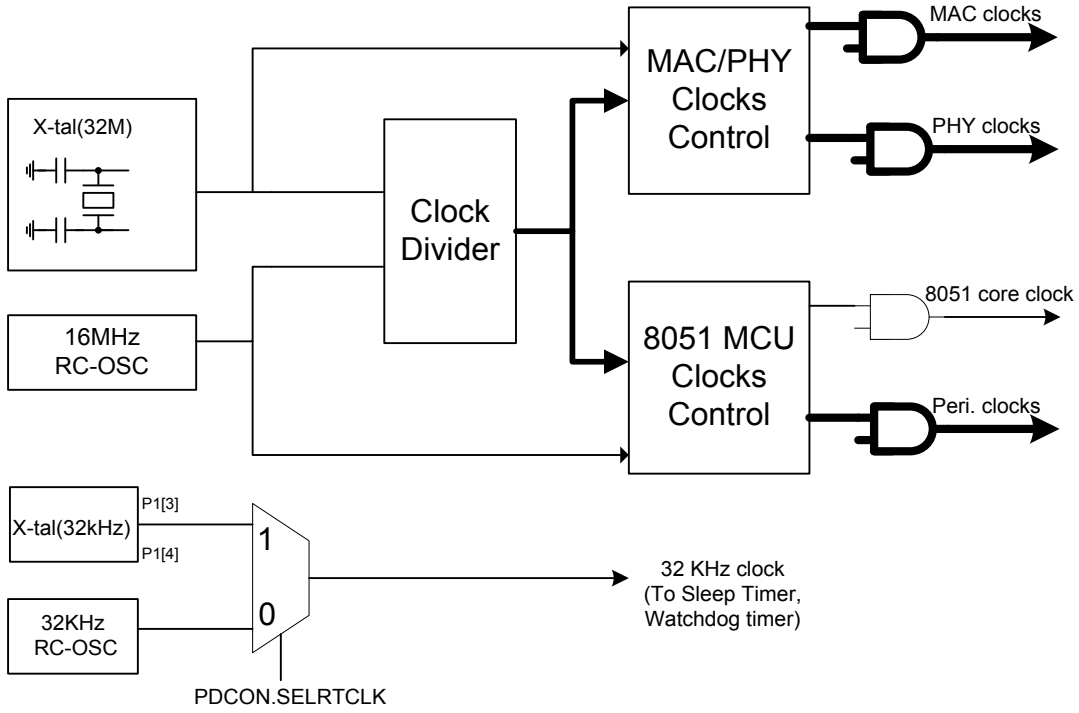



**Figure 7. Clock System Overview**

Two high speed oscillators are included in the MG2471. One is 32 MHz crystal oscillator and the other is 16MHz RC oscillator (HSRCOSC). The high speed 32MHz crystal oscillator startup time may be too long for the power critical applications. For example, the wake-up time from the power down mode is longer than the RC oscillator. So, the MG2471 can run on the 16MHz RC oscillator until the 32MHz crystal oscillator is stable.

### 7.2.1. 8051 MCU Reference Clock Control

The 8 MHz clock source from 32MHz crystal and a high-speed RC oscillator can be used to drive the internal 8051 MCU clock in MG2471. The default clock frequency of MG2471 is 8 MHz. When selecting 8051 MCU clock, the SFR CLKCON1 should be set as follows;

**MCU subsystem Reference Clock Control 1 (CLKCON1, 0x8E)**

<table>
<tr><th>Bit Field</th><th>Name</th><th>Descriptions</th><th>RW</th><th>Reset Value</th></tr>
<tr><td>7</td><td>CLK8M_DIV[2]</td><td rowspan="3"><table><tr><th>Value</th><th>CLK8M divider ratio</th></tr><tr><td>000</td><td>CLK8M is divided by 1(8MHz)</td></tr><tr><td>001</td><td>CLK8M/2(4MHz)</td></tr><tr><td>010</td><td>CLK8M/4(2MHz)</td></tr><tr><td>011</td><td>CLK8M/8(1MHz)</td></tr><tr><td>100</td><td>CLK8M/32(0.25 MHz)</td></tr><tr><td>101</td><td>CLK8M/512(15.625 KHz)</td></tr><tr><td>110</td><td>CLK8M/4096(1.953 KHz)</td></tr><tr><td>111</td><td>CLK8M/16384(488 Hz)</td></tr></table></td><td rowspan="3">R/W</td><td rowspan="3">000</td></tr>
<tr><td>6</td><td>CLK8M_DIV[1]</td></tr>
<tr><td>5</td><td>CLK8M_DIV[0]</td></tr>
<tr><td>4</td><td>HSRCOSC_SEL</td><td>HS RCOSC selection<br>1: the clock selected is the HS RCOSC source<br>0: the clock selection depends on CLK16M_SEL bit.</td><td>R/W</td><td>0</td></tr>
<tr><td>3</td><td>CLK16M_SEL</td><td>16MHz clock selection bit<br>1: 16MHz from 32MHz crystal is selected,<br>0: 8MHz from 32MHz crystal is selected</td><td>R/W</td><td>0</td></tr>
<tr><td>2</td><td>CLK16M_DIV[2]</td><td rowspan="3"><table><tr><th>Value</th><th>CLK16M divider ratio</th></tr><tr><td>000</td><td>CLK16M is divided by 1(16 MHz)</td></tr><tr><td>001</td><td>CLK16M/2(8 MHz)</td></tr><tr><td>010</td><td>CLK16M/4(4 MHz)</td></tr><tr><td>011</td><td>CLK16M/8(2 MHz)</td></tr><tr><td>100</td><td>CLK16M/32(0.5 MHz)</td></tr><tr><td>101</td><td>CLK16M/512(31.25 KHz)</td></tr><tr><td>110</td><td>CLK16M/4096(3.906 KHz)</td></tr><tr><td>111</td><td>CLK16M/16384(976 Hz)</td></tr></table></td><td rowspan="3">R/W</td><td rowspan="3">000</td></tr>
<tr><td>1</td><td>CLK16M_DIV[1]</td></tr>
<tr><td>0</td><td>CLK16M_DIV[0]</td></tr>
</table>

**MCU subsystem Reference Clock Control 2(CLKCON2, 0x8F)**

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| 7 | MCU_INIT_WAIT | This bit is the status flag for detecting the MCU internal clock state change. | RO | 0 |
| 6 | HSRCOSC_STS | When the MG2471 is gone into the power-down mode, this bit is set to 1. The HS RCOSC source is used as the wake-up clock when exiting from the power-down mode. In order to return to the normal mode, this bit should be cleared by SFR write operation to CLKCON2. | R/W | 0 |
| 5:0 | Reserved | This value read from this bits is 0 | RO | 0 |

The 8051 MCU clock should be changed to normal clock sources after wake-up from a

power-down mode by SFR CLKCON2 register writing. Please take care of this register setting.

### 7.2.2. MCU Peripherals Clock Control

The operating clock of 8051 MCU peripherals can be enabled or disabled by some SFR registers write operation. For details, please refer to the SFRs description below.

**Peripheral Clock Stop 0(PERI_CLK_STP0, 0x98)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | SPI_ON | This bit is for enabling or disabling the operating clock of SPI.<br>0 : clock is off<br>1 : clock is on | R/W | 0 |
| 6 | UART1_ON | This bit is for enabling or disabling the operating clock of UART1.<br>0 : clock is off<br>1 : clock is on | R/W | 1 |
| 5 | UART0_ON | This bit is for enabling or disabling the operating clock of UART0.<br>0 : clock is off<br>1 : clock is on | R/W | 1 |
| 4 | GPIO_ON | This bit is for enabling or disabling the operating clock of GPIO.<br>0 : clock is off<br>1 : clock is on | R/W | 1 |
| 3 | TIMER3_ON | This bit is for enabling or disabling the operating clock of TIMER 3<br>0 : clock is off<br>1 : clock is on | R/W | 0 |
| 2 | TIMER2_ON | This bit is for enabling or disabling the operating clock of TIMER 2.<br>0 : clock is off<br>1 : clock is on | R/W | 0 |
| 1 | TIMER1_ON | This bit is for enabling or disabling the operating clock of TIMER 1.<br>0 : clock is off<br>1 : clock is on | R/W | 0 |
| 0 | TIMER0_ON | This bit is for enabling or disabling the operating clock of TIMER 0.<br>0 : clock is off<br>1 : clock is on | R/W | 0 |

**Peripheral Clock Stop 1(PERI_CLK_STP1, 0x99)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | I2C_ON | This bit is for enabling or disabling the operating clock of I2C controller.<br>0 : clock is off<br>1 : clock is on | R/W | 0 |
| 6 | IRTX_ON | This bit is for enabling or disabling the operating clock of IR TX modulator.<br>0 : clock is off | R/W | 0 |

| | | | | |
|---|---|---|---|---|
| | | 1 : clock is on | | |
| 5 | FLASHC_ON | This bit is for enabling or disabling the operating clock of flash controller.<br>0 : clock is off<br>1 : clock is on | R/W | 0 |
| 4 | I2SFIFO_ON | This bit is for enabling or disabling the operating clock of I2S FIFO block.<br>0 : clock is off<br>1 : clock is on | R/W | 0 |
| 3 | I2SRX_ON | This bit is for enabling or disabling the operating clock of I2S RX.<br>0 : clock is off<br>1 : clock is on | R/W | 0 |
| 2 | I2STX_ON | This bit is for enabling or disabling the operating clock of I2S TX.<br>0 : clock is off<br>1 : clock is on | R/W | 0 |
| 1 | QUAD_ON | This bit is for enabling or disabling the operating clock of quadrature signal decoder.<br>0 : clock is off<br>1 : clock is on | R/W | 0 |
| 0 | RNG_ON | This bit is for enabling or disabling the operating clock of random number generator.<br>0 : clock is off<br>1 : clock is on | R/W | 0 |

**Peripheral Clock Stop 2(PERI_CLK_STP2, 0x9A)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | PWM_CH4_ON | This bit is for enabling or disabling the operating clock of PWM channel 4.<br>0 : clock is off<br>1 : clock is on | R/W | 0 |
| 6 | PWM_CH3_ON | This bit is for enabling or disabling the operating clock of PWM channel 3.<br>0 : clock is off<br>1 : clock is on | R/W | 0 |
| 5 | PWM_CH2_ON | This bit is for enabling or disabling the operating clock of PWM channel 2.<br>0 : clock is off<br>1 : clock is on | R/W | 0 |
| 4 | PWM_CH1_ON | This bit is for enabling or disabling the operating clock of PWM channel 1.<br>0 : clock is off<br>1 : clock is on | R/W | 0 |
| 3 | PWM_CH0_ON | This bit is for enabling or disabling the operating clock of PWM channel 0.<br>0 : clock is off<br>1 : clock is on | R/W | 0 |
| 2 | MPTOP_ON | This bit is for enabling or disabling the operating clock of MAC/PHY registers interface block. | R/W | 1 |

| | | | | |
|---|---|---|---|---|
| | | 0 : clock is off<br>1 : clock is on | | |
| 1 | LOGIC3V_ON | This bit is for enabling or disabling the operating clock of LOGIC3V registers interface block.<br>0 : clock is off<br>1 : clock is on | R/W | 1 |
| 0 | CLKRST_CTL_ON | This bit is for enabling or disabling the operating clock of clock & reset controller.<br>0 : clock is off<br>1 : clock is on | R/W | 1 |

**Peripheral Clock Stop 3(PERI_CLK_STP3, 0x92)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:4 | | Reserved | RO | 0 |
| 3 | P3_INTCTL_ON | This bit is for enabling or disabling the operating clock of the interrupt controller for the external P3[1:0]/P3[7:4] pins.<br>0 : clock is off<br>1 : clock is on | R/W | 0 |
| 2 | P1_INTCTL_ON | This bit is for enabling or disabling the operating clock of the interrupt controller for the external P1[1:0]/P1[4:3]/P1[7:6] pins .<br>0 : clock is off<br>1 : clock is on | R/W | 0 |
| 1 | P0_INTCTL_ON | This bit is for enabling or disabling the operating clock of the interrupt controller for the external P0[7:0] pins .<br>0 : clock is off<br>1 : clock is on | R/W | 0 |
| 0 | WDT_ON | This bit is for enabling or disabling the operating clock of Watchdog timer block.<br>0 : clock is off<br>1 : clock is on | R/W | 1 |

### 7.2.3. MAC/PHY Clocks Control

Please refer to the clock & reset in Sec 8.1 of peripherals chapter for details.

## 7.3. Resets

The MG2471 has four types of reset sources.

- The external pin RESETB is inputted to low during more than 62.5 us
- Internal POR(Power-On-Reset) condition
- Internal BOD(Brown Out Detector) reset condition
- Watchdog timer reset condition

The initial conditions after a reset are as follows;

- I/O pins are configured as inputs with pull-up
- CPU program counter is loaded with 0x0000 and program execution starts at this address
- All peripheral registers are initialized to their reset values.
- Watchdog timer is enabled

The resets of MAC/PHY blocks are controlled by the separate reset controller block in the MG2471. They can be reset by S/W control besides four sources for system reset. For more detailed information, please refer to the register description in the clock & reset controller(Sec 8.1).

## 7.4. Interrupts

The 8051 MCU of MG2471 employs a program interrupt method similar to the one of other MCU. When the interrupt event occurs, the 8051 CPU core jumps to the location which is called as an interrupt vector address and the interrupt service routine at the corresponding vector address is executed. When the interrupt subroutine completes, execution resumes at the point where the interrupt occurred. Interrupts can occur as a result of internal activity (e.g. timer0 overflow) or at the initiation of an external device (external interrupt pin). All the interrupts of MG2471 can be enabled or disabled dynamically by a user.

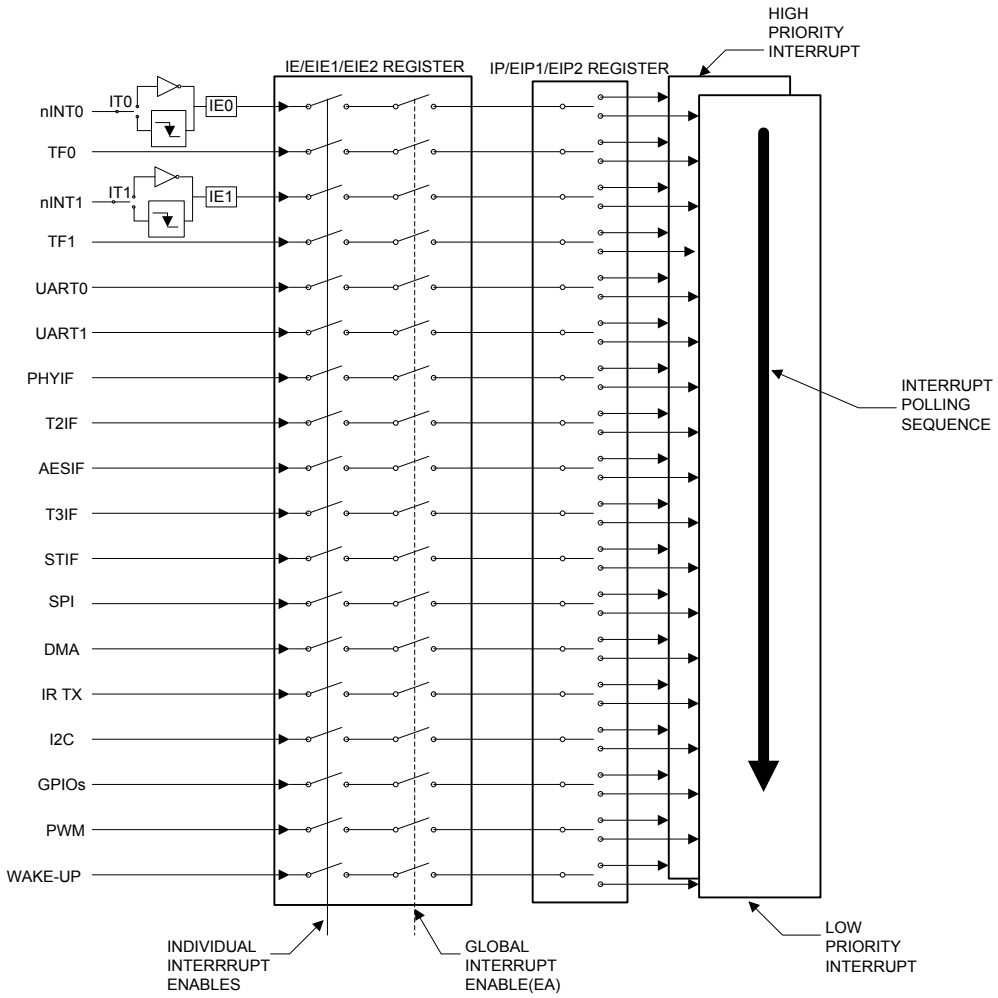



**Figure 8. Interrupts Overview of MG2471**

MG2471 has 18 interrupt sources. [Table 5] describes the detailed information for each of the interrupt sources. The ‘Interrupt Address’ indicates the address where the interrupt service routine is located. The ‘Interrupt Flag’ is the bit that notifies the MCU that the corresponding interrupt has occurred. ‘Interrupt Enable’ is the bit which decides whether each interrupt has been enabled. ‘Interrupt Priority’ is the bit which decides the priority of the interrupt. ‘Interrupt Number’ is the interrupt priority fixed by the hardware. That is, when two or more interrupts having the same ‘Interrupt Priority’ value, occur simultaneously, the lower ‘Interrupt Number’ is processed first.

**Table 5. Interrupt Descriptions**

| Interrupt Number | Interrupt Type | Interrupt Address | Interrupt Flag | Interrupt Enable | Interrupt Priority |
|---|---|---|---|---|---|
| 0 | External Interrupt0 | 0x0003 | TCON.IE0 (TCON[1]) | IE.EX0 (IE[0]) | IP[0] |
| 1 | Timer0 Interrupt | 0x000B | TCON.TF0 (TCON[5]) | IE.ET0 (IE[1]) | IP[1] |
| 2 | External Interrupt1 | 0x0013 | TCON.IE1 (TCON[3]) | IE.EX1 (IE[2]) | IP[2] |
| 3 | Timer1 Interrupt | 0x001B | TCON.TF1 (TCON[7]) | IE.ET1 (IE[3]) | IP[3] |
| 4 | UART0 Interrupt | 0x0023 | Refer to Note1 | IE.ES0 (IE[4]) | IP[4] |
| 5 | IR TX Interrupt | 0x002B | Refer to Note2 | EIE2[0] | EIP2[0] |
| 6 | I2C Interrupt | 0x0033 | Refer to Note3 | EIE2[1] | EIP2[1] |
| 7 | UART1 Interrupt | 0x003B | Refer to Note1 | IE.ES1 (IE[6]) | IP[6] |
| 8 | PHY Interrupt | 0x0043 | Refer to Note4 | EIE1.PHYIE (EIE1[0]) | EIP1[0] |
| 9 | Timer2 Interrupt | 0x004B | EXIF1.T2IF (EXIF1[5]) | EIE1.T2IE (EIE1[1]) | EIP1[1] |
| 10 | AES Done Interrupt | 0x0053 | EXIF1.AESIF (EXIF1[6]) | EIE1.AESIE (EIE1[2]) | EIP1[2] |
| 11 | Timer3 Interrupt | 0x005B | EXIF1.T3IF (EXIF1[7]) | EIE1.T3IE (EIE1[3]) | EIP1[3] |
| 12 | Sleep-Timer time-out Interrupt | 0x0063 | EXIF2.STIF (EXIF2[1]) | EIE1.STIE (EIE1[4]) | EIP1[4] |
| 13 | SPI Interrupt | 0x006B | Refer to Note5 | EIE1.SPIIE (EIE1[5]) | EIP1[5] |
| 14 | DMA Interrupt | 0x0073 | Refer to Note6 | EIE1.DMAIE (EIE1[6]) | EIP1[6] |
| 15 | Wake-up Interrupt | 0x007B | EXIF2.WUIF (EXIF2[0]) | EIE1.WUIE (EIE1[7]) | EIP1[7] |
| 16 | GPIO Interrupt | 0x0083 | Refer to Note7 | EIE2[2] | EIP2[2] |
| 17 | PWM Interrupt | 0x008B | Refer to Note8 | EIE2[3] | EIP2[3] |

***Note 1:*** *In case of a UART Interrupt, bit[0] of the IIR register(0x2502,0x2512) in the UART block is used as a flag. Also, the Tx, Rx, Timeout, Line Status and Modem Status interrupts can be distinguished by bit[3:1] value. For more detailed information, refer to the UART0/1 description in Sec 8.7.*

***Note 2:*** *In case of an IR TX interrupt, please refer to the IR Modulator section (8.10)*

***Note 3:*** *In case of an I2C interrupt, please refer to the I2C section (8.9)*

***Note 4:*** *In case of an PHY interrupt, please refer to the section (9.2.1) of PHY chapter.*

***Note 5:*** *In case of an SPI interrupt, there is another interrupt enable bit in the SPI register besides EIE.SPIIE. In order to enable SPI interrupt, both SPIE in SPCR (0x2540) register and EIE.SPIIE should be set to '1'. And, SPIF in SPSR (0x2541) register acts as an interrupt flag.*

***Note 6:*** *In case of a DMA interrupt, there are interrupt enable register and interrupt flag register in I2S FIFO block. The interrupt enable register are VTFINTENA (0x2770), VRFINTENA (0x2771) and VDMINTENA (0x2772). There are 24 interrupt sources. When both an interrupt enable signal and an interrupt flag signal are set to '1,' DMA interrupt is enabled.*

***Note 7:*** *In case of a GPIO interrupt, please refer to the GPIO section (8.2).*

***Note 8:*** *In case of a PWM interrupt, please refer to the PWM section (8.5).*

### 7.4.1. Interrupt Sources

The MG2471 has the 18 hardware interrupt sources. They include two external interrupts (nINT0/P3[2] & nINT1/P3[3]), four timer interrupts(timer 0/1/2/3), two UART interrupts and ten additional interrupts. Each interrupt has an interrupt request flag and for some interrupts, hardware clears the request flag when it grants an interrupt. The followings are interrupt sources in the MG2471.

- External interrupts(IE0 and IE1 in TCON register)
- PHY interrupt
- AES done interrupt
- Sleep timer time-out interrupt
- MCU peripherals interrupt
  - ✓ Timer 0&1 (TF0 and TF1 in TCON register)
  - ✓ Timer 2&3 (T2IF and T3IF in EXIF register)
  - ✓ UART0 & UART1
  - ✓ SPI
  - ✓ DMA
  - ✓ 5-channel PWM
  - ✓ IR modulator
  - ✓ I2C
  - ✓ All GPIO pins except P3[3:2] pins under normal mode
  - ✓ Two external interrupt sources P3[3:2] pins
    (Theses can be used as wakeup sources under the power down mode.)
- Wake-up interrupt from the power-down mode

**EXTENDED INTERRUPT FLAG REGISTER 1 (EXIF1, 0x91)**

This register stores the interrupt state corresponding to each bit. When the interrupt corresponding to a bit is triggered, the flag is set to '1'.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | T3IF | Timer3 Interrupt Flag.<br>0: No interrupt<br>1: Interrupt pending<br>*Note: To clear the interrupt flag, The 1 must be written into this bit. | R/W | 0 |
| 6 | AESIF | AES Interrupt Flag.<br>0: No interrupt<br>1: Interrupt pending<br>*Note: To clear the interrupt flag, The 1 must be written into this bit | R/W | 0 |
| 5 | T2IF | Timer2 Interrupt Flag.<br>0: No interrupt<br>1: Interrupt pending<br>*Note: To clear the interrupt flag, The 1 must be written into this bit. | R/W | 0 |
| 4:0 | | Reserved bits | RO | 0 |

**EXTENDED INTERRUPT FLAG REGISTER 2 (EXIF2, 0xD8)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:2 | | Reserved | RO | 0 |
| 1 | STIF | Sleep timer time-out interrupt flag under normal mode.<br>0: No interrupt<br>1: Interrupt pending<br>*Note: To clear the interrupt flag, 1 must be written into this bit. | R/W | 0 |
| 0 | WUIF | Power-down wake-up interrupt flag<br>0: No interrupt<br>1: Interrupt pending<br>*Note: To clear the interrupt flag, 1 must be written into this bit. | R/W | 0 |

### 7.4.2. Interrupt Enable

The EA bit in the IE register is the global interrupt enable signal for all interrupts. In addition, each interrupt is masked by each interrupt enable bit. Therefore, in order to use an interrupt, both EA and the specific interrupt enable bit should be set to '1'. When the bit for each interrupt is '0', that interrupt is disabled. When the bit for each interrupt is '1', that interrupt is

enabled.

**Interrupt Enable Register (IE, 0xA8)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | EA | Global interrupt enable<br>0: No interrupt will be acknowledged.<br>1: Each interrupt source is individually enabled or disabled by setting its corresponding enable bit. | R/W | 0 |
| 6 | ES1 | UART1 interrupt enable<br>0: interrupt disabled<br>1: interrupt enabled<br>(EA bit should be set to '1') | R/W | 0 |
| 5 | | Reserved | RO | 0 |
| 4 | ES0 | UART0 interrupt enable<br>0: interrupt disabled<br>1: interrupt enabled<br>(EA bit should be set to '1') | R/W | 0 |
| 3 | ET1 | Timer1 interrupt enable<br>0: interrupt disabled<br>1: interrupt enabled<br>(EA bit should be set to '1') | R/W | 0 |
| 2 | EX1 | External interrupt1 enable<br>0: interrupt disabled<br>1: interrupt enabled<br>(EA bit should be set to '1') | R/W | 0 |
| 1 | ET0 | Timer0 interrupt enable<br>0: interrupt disabled<br>1: interrupt enabled<br>(EA bit should be set to '1') | R/W | 0 |
| 0 | EX0 | External interrupt0 enable<br>0: interrupt disabled<br>1: interrupt enabled<br>(EA bit should be set to '1') | R/W | 0 |

**Extended Interrupt Enable Register 1(EIE1, 0xE8)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | WUIE | Wake-up from the power-down mode interrupt enable<br>0: interrupt disabled | R/W | 0 |

| | | | | |
|---|---|---|---|---|
| | | 1: interrupt enabled | | |
| 6 | DMAIE | DMA interrupt enable<br>0: interrupt disabled<br>1: interrupt enabled | R/W | 0 |
| 5 | SPIIE | SPI interrupt enable<br>0: interrupt disabled<br>1: interrupt enabled | R/W | 0 |
| 4 | STIE | Sleep Timer Time-out interrupt enable<br>0: interrupt disabled<br>1: interrupt enabled | R/W | 0 |
| 3 | T3IE | Timer3 interrupt enable<br>0: interrupt disabled<br>1: interrupt enabled | R/W | 0 |
| 2 | AESIE | AES Done interrupt enable<br>0: interrupt disabled<br>1: interrupt enabled | R/W | 0 |
| 1 | T2IE | Timer2 interrupt enable<br>0: interrupt disabled<br>1: interrupt enabled | R/W | 0 |
| 0 | PHYIE | PHY interrupt enable<br>0: interrupt disabled<br>1: interrupt enabled | R/W | 0 |

**Extended Interrupt Enable Register 2(EIE2, 0xE9)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:4 | | Reserved bits | RO | 0 |
| 3 | EIE2[3] | PWM interrupt enable<br>0: interrupt disabled<br>1: interrupt enabled | R/W | 0 |
| 2 | EIE2[2] | GPIO interrupt enable<br>0: interrupt disabled<br>1: interrupt enabled | R/W | 0 |
| 1 | EIE2[1] | I2C interrupt enable<br>0: interrupt disabled<br>1: interrupt enabled | R/W | 0 |
| 0 | EIE2[0] | IR TX interrupt enable<br>0: interrupt disabled<br>1: interrupt enabled | R/W | 0 |

### 7.4.3. Interrupt Priority

Each interrupt source can also be individually programmed to one of two priority levels by setting or clearing a bit in SFRs IP/EIP1/EIP2. A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

**INTERRUPT PRIORITY REGISTER (IP, 0xB8)**

If a bit corresponding to each interrupt is '0', the corresponding interrupt has lower priority and if a bit is '1', the corresponding interrupt has higher priority.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | | Reserved | RO | 0 |
| 6 | PS1 | UART1 interrupt priority bit<br>0: assign low priority<br>1: assign high priority | R/W | 0 |
| 5 | | Reserved | RO | 0 |
| 4 | PS0 | UART 0 interrupt priority bit<br>0: assign low priority<br>1: assign high priority | R/W | 0 |
| 3 | PT1 | Timer1 interrupt priority bit<br>0: assign low priority<br>1: assign high priority | R/W | 0 |
| 2 | PX1 | External interrupt1 interrupt priority bit<br>0: assign low priority<br>1: assign high priority | R/W | 0 |
| 1 | PT0 | Timer0 interrupt priority bit<br>0: assign low priority<br>1: assign high priority | R/W | 0 |
| 0 | PX0 | External interrupt0 interrupt priority bit<br>0: assign low priority<br>1: assign high priority | R/W | 0 |

**EXTENDED INTERRUPT PRIORITY REGISTER 1 (EIP1, 0xF8)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | | Reserved | RO | 0 |
| 6 | DMAIP | DMA interrupt priority bit<br>1: DMA interrupt has higher priority.<br>0: DMA interrupt has lower priority. | R/W | 0 |
| 5 | SPIIP | SPI interrupt priority bit<br>1: PI interrupt has higher priority.<br>0: PI interrupt has lower priority. | R/W | 0 |

| | | | | |
|---|---|---|---|---|
| 4 | RTCIP | Sleep Timer time-out interrupt priority bit<br>1: Sleep Timer interrupt has higher priority.<br>0: Sleep Timer interrupt has lower priority. | R/W | 0 |
| 3 | T3IP | Timer3 interrupt priority bit<br>1: Timer3 interrupt has higher priority.<br>0: Timer3 interrupt has lower priority. | R/W | 0 |
| 2 | AESIP | AES interrupt priority bit<br>1: AES interrupt has higher priority.<br>0: AES interrupt has lower priority. | R/W | 0 |
| 1 | T2IP | Timer2 interrupt priority bit<br>1: Timer2 interrupt has higher priority.<br>0: Timer2 interrupt has lower priority. | R/W | 0 |
| 0 | PHYIP | PHY interrupt priority bit<br>1: PHY interrupt has higher priority.<br>0: PHY interrupt has lower priority. | R/W | 0 |

**EXTENDED INTERRUPT PRIORITY REGISTER 2 (EIP2, 0xF9)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:4 | | Reserved bits | RO | 0 |
| 3 | PWMIP | PWM interrupt priority bit<br>1: PWM interrupt has higher priority.<br>0: PWM interrupt has lower priority. | R/W | 0 |
| 2 | GPIOIP | GPIO interrupt priority bit<br>1: GPIO interrupt has higher priority.<br>0: GPIO interrupt has lower priority. | R/W | 0 |
| 1 | I2CIP | I2C interrupt priority bit<br>1: I2C interrupt has higher priority.<br>0: I2C interrupt has lower priority. | R/W | 0 |
| 0 | IRTXIP | IR TX interrupt priority<br>1: IR TX interrupt has higher priority.<br>0: IR TX interrupt has lower priority. | R/W | 0 |

# 8. PERIPHERALS

## 8.1. Clock and Reset Controller

This block supports the clock on/off and SW resets for the individual blocks in the MAC/PHY or RF/Analog. Also, it selects the ADC sampling clock of ADC decimator block and controls the clock output function for supplying the clock to external devices.

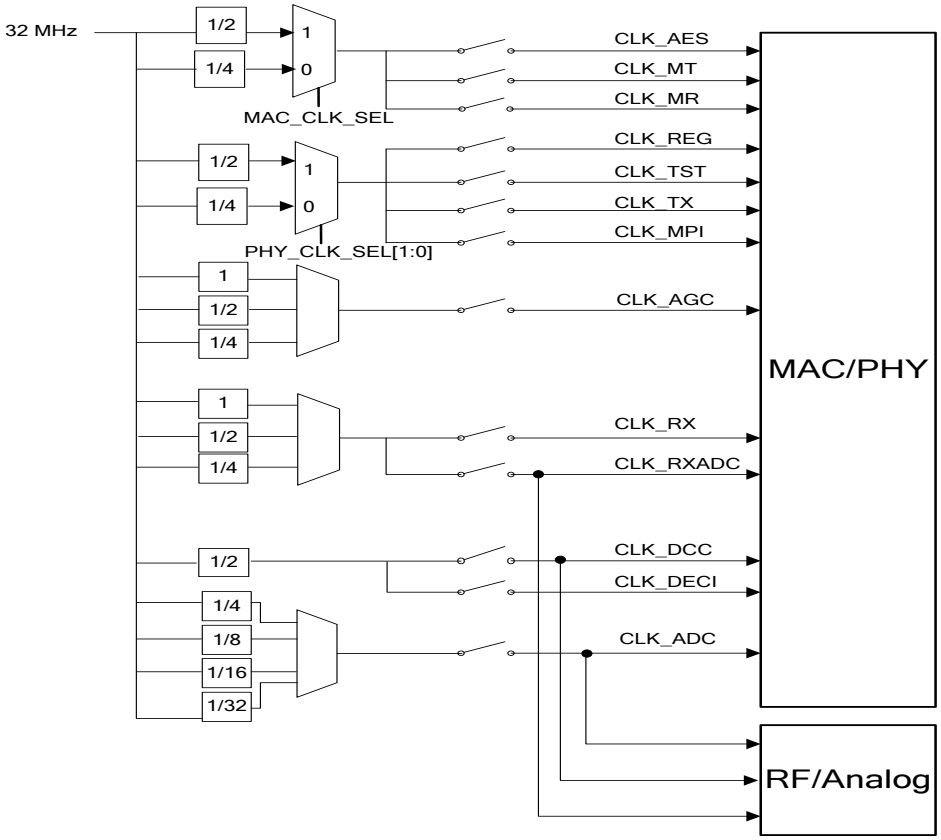



**Figure 9. Clocks Structure of the MAC/PHY block**

**PHY_CLK_EN0 (PHY Clock Enable Register 0, 0x2780)**
This register is used to enable or disable clocks of the MAC/PHY block.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | CLK_MPI_EN | CLK_MPI clock on/off control bit<br>0: clock disabled<br>1: clock enabled | R/W | 0 |
| 6 | CLK_RX_EN | CLK_RX clock on/off control bit<br>0: clock disabled<br>1: clock enabled | R/W | 0 |
| 5 | CLK_REG_EN | CLK_REG clock on/off control bit<br>0: clock disabled<br>1: clock enabled | R/W | 1 |

| | | | | |
|---|---|---|---|---|
| 4 | CLK_TX_EN | CLK_TX clock on/off control bit<br>0: clock disabled<br>1: clock enabled | R/W | 0 |
| 3 | CLK_TST_EN | CLK_TST clock on/off control bit<br>0: clock disabled<br>1: clock enabled | R/W | 0 |
| 2 | CLK_MR_EN | CLK_MR clock on/off control bit<br>0: clock disabled<br>1: clock enabled | R/W | 0 |
| 1 | CLK_MT_EN | CLK_MT clock on/off control bit<br>0: clock disabled<br>1: clock enabled | R/W | 0 |
| 0 | CLK_AES_EN | CLK_AES clock on/off control bit<br>0: clock disabled<br>1: clock enabled | R/W | 0 |

**PHY_CLK_EN1 (PHY Clock Enable Register 1, 0x2781)**

This register is used to enable or disable clocks of the MAC/PHY or RF/Analog block.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:6 | | Reserved | RO | 0 |
| 5 | DCCLK_EN | DCCLK (16MHz) clock on/off control bit<br>0: clock disabled<br>1: clock enabled | R/W | 0 |
| 4 | CLK_32M_EN | 32 MHz clock on/off control bit for just monitoring<br>0: clock disabled<br>1: clock enabled | R/W | 0 |
| 3 | CLK_ADC_EN | CLK_ADC clock on/off control bit<br>0: clock disabled<br>1: clock enabled | R/W | 0 |
| 2 | CLK_DECI_EN | CLK_DECI clock on/off control bit<br>0: clock disabled<br>1: clock enabled | R/W | 0 |
| 1 | CLK_DMCAL_EN | CLK_DMCAL clock on/off control bit<br>0: clock disabled<br>1: clock enabled | R/W | 0 |
| 0 | CLK_RXADC_EN | CLK_RXADC clock on/off control bit<br>0: clock disabled<br>1: clock enabled | R/W | 0 |

**PHY_CLK_FR_EN0 (PHY Clock Force Enable Register 0, 0x2782)**

This register is always used to enable the clock regardless of clock enable registers setting.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | CLK_MPI_FR_EN | Force the CLK_MPI clock to be enabled regardless of CLK_MPI_EN bit setting<br>0: clock is not forced to be enabled<br>1: clock is forced to be enabled | R/W | 0 |
| 6 | CLK_RX_FR_EN | Force the CLK_RX clock to be enabled regardless of CLK_RX_EN bit setting<br>0: clock is not forced to be enabled<br>1: clock is forced to be enabled | R/W | 0 |
| 5 | CLK_REG_FR_EN | Force the CLK_REG clock to be enabled regardless of CLK_REG_EN bit setting<br>0: clock is not forced to be enabled<br>1: clock is forced to be enabled | R/W | 0 |
| 4 | CLK_TX_FR_EN | Force the CLK_TX clock to be enabled regardless of CLK_TX_EN bit setting<br>0: clock is not forced to be enabled<br>1: clock is forced to be enabled | R/W | 0 |
| 3 | CLK_TST_FR_EN | Force the CLK_TST clock to be enabled regardless of CLK_TST_EN bit setting<br>0: clock is not forced to be enabled<br>1: clock is forced to be enabled | R/W | 0 |
| 2 | CLK_MR_FR_EN | Force the CLK_MR clock to be enabled regardless of CLK_MR_EN bit setting<br>0: clock is not forced to be enabled<br>1: clock is forced to be enabled | R/W | 0 |
| 1 | CLK_MT_FR_EN | Force the CLK_MT clock to be enabled regardless of CLK_MT_EN bit setting<br>0: clock is not forced to be enabled<br>1: clock is forced to be enabled | R/W | 0 |
| 0 | CLK_AES_FR_EN | Force the CLK_AES clock to be enabled regardless of CLK_AES_EN bit setting<br>0: clock is not forced to be enabled<br>1: clock is forced to be enabled | R/W | 0 |

**PHY_CLK_FR_EN1 (PHY Clock Force Enable Register 1, 0x2783)**

This register is always used to enable the clock regardless of clock enable registers setting.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:6 | | Reserved | RO | 0 |
| 5 | DCCLK_FR_EN | Force the DCCLK clock to be enabled regardless of DCCLK_EN bit setting<br>0: clock is not forced to be enabled | R/W | 0 |

| | | | | |
|---|---|---|---|---|
| | | 1: clock is forced to be enabled | | |
| 4 | OSCLK_FR_EN | Force the OSCLK clock to be enabled regardless of OSCLK_EN bit setting<br>0: clock is not forced to be enabled<br>1: clock is forced to be enabled | R/W | 0 |
| 3 | CLK_ADC_FR_EN | Force the CLK_ADC clock to be enabled regardless of CLK_ADC_EN bit setting<br>0: clock is not forced to be enabled<br>1: clock is forced to be enabled | R/W | 0 |
| 2 | CLK_DECI_FR_EN | Force the CLK_DECI clock to be enabled regardless of CLK_DECI_EN bit setting<br>0: clock is not forced to be enabled<br>1: clock is forced to be enabled | R/W | 0 |
| 1 | CLK_DMCAL_FR_EN | Force the CLK_DMCAL clock to be enabled regardless of CLK_DMCAL_EN bit setting<br>0: clock is not forced to be enabled<br>1: clock is forced to be enabled | R/W | 0 |
| 0 | CLK_RXADC_FR_EN | Force the CLK_RXADC clock to be enabled regardless of CLK_RXADC_EN bit setting<br>0: clock is not forced to be enabled<br>1: clock is forced to be enabled | R/W | 0 |

**PHY_SW_RSTB (PHY S/W Reset Register, 0x2784)**

This register is used to control the S/W resets of the MAC/PHY block. The active reset level is low.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | | Reserved | RO | 1 |
| 6 | RESETB_DECI | RESETB_DECI reset signal control bit<br>0: RESETB_DECI active<br>1: RESETB_DECI inactive | R/W | 1 |
| 5 | RESETB_MAC | RESETB_MAC reset signal control bit<br>0: RESETB_MAC active<br>1: RESETB_MAC inactive | R/W | 1 |
| 4 | RESETB_MPI | RESETB_MPI reset signal control bit<br>0: RESETB_MPI active<br>1: RESETB_MPI inactive | R/W | 1 |
| 3 | RESETB_REG | RESETB_REG reset signal control bit<br>0: RESETB_REG active<br>1: RESETB_REG inactive | R/W | 1 |
| 2 | RESETB_RF | RESETB_RF reset signal control bit<br>0: RESETB_RF active<br>1: RESETB_RF inactive | R/W | 1 |
| 1 | RESETB_TX | RESETB_TX reset signal control bit | R/W | 1 |

| | | | | |
|---|---|---|---|---|
| | | 0: RESETB_TX active<br>1: RESETB_TX inactive | | |
| 0 | RESETB_RX | RESETB_RX reset signal control bit<br>0: RESETB_RX active<br>1: RESETB_RX inactive | R/W | 1 |

**MPTOP_CLK_SEL (MAC/PHY Clock Selection Register, 0x2785)**

This register selects the operating clock of the MAC/PHY block depending on the selected data rate mode.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:4 | | Reserved bits | RO | 0 |
| 3 | CLK_AGC_SEL | Select the operating frequency of internal CLK_AGC clock source<br>**Data Rate** / **Bit value**<br>2Mcps: 0: 8 MHz, 1: 16 MHz<br>4Mcps: 0: 16 MHz, 1: 32 MHz | R/W | 0 |
| 2 | MAC_CLK_SEL | Select the operating frequency of MAC block<br>0 : 8MHz<br>1 : 16MHz | R/W | 0 |
| 1 | PHY_CLK_SEL[1] | **Bit values** / **Configuration**<br>11: 4Mcps clocks selection<br>others: 2Mcps clocks selection | R/W | 0 |
| 0 | PHY_CLK_SEL[0] | | R/W | 0 |

**ADC_CLK_SEL (ADC Sampling Clock Selection Register, 0x2786)**

This register selects the ADC sampling clock to ADC decimator block.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:2 | | Reserved | RO | 0 |
| 1 | ADC_CLK_SEL[1] | **Bit values** / **ADC sampling clock**<br>00: 1 MHz<br>01: 2 MHz<br>10: 4 MHz<br>11: Not valid | R/W | 10 |
| 0 | ADC_CLK_SEL[0] | | | |

**EXT_CLK_CTL (External Clock Output Control Register, 0x2787)**

The MG2471 supports the external clock output function to interface with the external devices. The selectable clock is as following table and is output to P1[3] when the clock output function is enabled. The default value is the clock output disabled.

<table>
<tr><th>Bit Field</th><th>Name</th><th>Descriptions</th><th>R/W</th><th>Reset Value</th></tr>
<tr><td>7</td><td>EXT_CLK_EN</td><td>Enable the external clock output function<br>0: output is disabled<br>1: output is enabled</td><td>R/W</td><td>0</td></tr>
<tr><td>6:3</td><td></td><td>Reserved</td><td>RO</td><td>0</td></tr>
<tr><td>2</td><td>EXT_CLK_SEL[2]</td><td rowspan="3"><table><tr><th>Bits values</th><th>External clock frequency</th></tr><tr><td>000</td><td>500 KHz</td></tr><tr><td>001</td><td>1 MHz</td></tr><tr><td>010</td><td>2 MHz</td></tr><tr><td>011</td><td>4 MHz</td></tr><tr><td>100</td><td>8 MHz</td></tr><tr><td>101</td><td>16 MHz</td></tr><tr><td>110</td><td>32 MHz</td></tr><tr><td>111</td><td>Clock is the off-state</td></tr></table></td><td>R/W</td><td>0</td></tr>
<tr><td>1</td><td>EXT_CLK_SEL[1]</td><td>R/W</td><td>0</td></tr>
<tr><td>0</td><td>EXT_CLK_SEL[0]</td><td>R/W</td><td>0</td></tr>
</table>

## 8.2. Input/Output Ports(GPIO)

The MG2471 has 22 general purpose pins which have the following key features;

- General I/O pins with selectable direction for each bit
- Programmable pull-up/down control for each bit
- Driving strength control for each bit
- External input disabling function for each bit
- Interrupt generation from all GPIO pins except P3[3:2]
  (This function is valid under normal mode and assigned to the separate interrupt vector.)
- External interrupt capability of P3[3:2] pins
  (These lines can be used to wake up the MG2471 from power down modes.)
- Wakeup sources in power down modes
  (For more detailed description, please see to Sec 8.15. Power management)

The GPIO functions are listed in [Table 6]. [Figure 10] shows the block diagram of the GPIO. The GPIO pins after a reset are configured as inputs with pull-up.

**Table 6. PORT-0/1/3 Operation Truth Table**

| INPUTs | | | | OUTPUT |
|---|---|---|---|---|
| **OEN** | **I** | **PE** | **PS** | **PAD** |
| 0 | 0 | x | x | 0 |
| 0 | 1 | x | x | 1 |
| 1 | x | 0 | x | Hi-Z |
| 1 | x | 1 | 0 | Pull-down |
| 1 | x | 1 | 1 | Pull-up |

| DS | Current Spec. |
|---|---|
| 0 | Low-drive |
| 1 | High-drive |

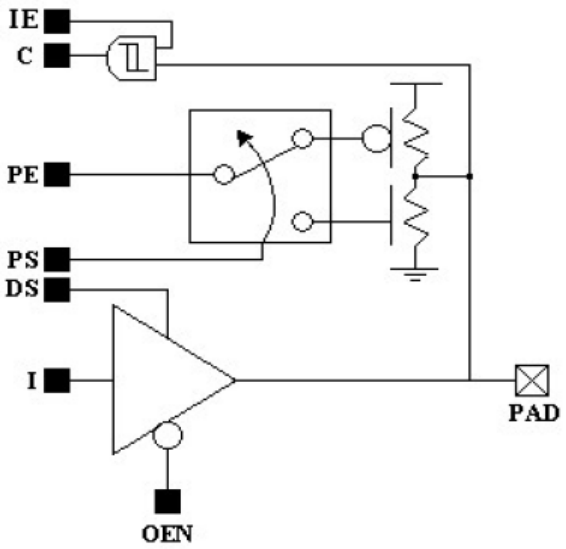



**Figure 10. PORT-0/1/3 PAD Block Diagram**

### 8.2.1. Port Data Registers(SFR area)

**PORT-3 DATA REGISTER (P3, 0xB0)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | P3[7:0] | This port register is used as a general purpose I/O ports.<br>When reading the each bit of PORT-3, the current status value of the corresponding bit is returned.<br>When writing the each bit of PORT-3, the corresponding PORT-3 bit is changed to the new value. By default, the direction of P3[7:0] is the input mode and the pull-up enable bit is the active-state.<br>For details of pull-up/pull-down controls of P3[7:0], Please see to the Power Management section(8.15). | R/W | Unknown |

**PORT-1 DATA REGISTER (P1, 0x90)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | P1[7:0] | This port register is used as a general purpose I/O ports.<br>When reading the each bit of PORT-1, the current status value of the corresponding bit is returned.<br>When writing the each bit of PORT-1, the corresponding PORT-1 bit is changed to the new value. By default, the direction of P1[7:0] is the input mode and the pull-up enable bit is the active-state.<br>For details of pull-up/pull-down controls of P1[7:0], Please see to the Power Management section(8.15).<br>*Note: The P1[2] and P1[5] are reserved bits. | R/W | Unknown |

**PORT-0 DATA REGISTER (P0, 0x80)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | P0[7:0] | This port register is used as a general purpose I/O ports.<br>When reading the each bit of PORT-0, the current status value of the corresponding bit is returned.<br>When writing the each bit of PORT-0, the corresponding PORT-0 bit is changed to the new value. By default, the direction of P0[7:0] is the input mode and the pull-up enable bit is the active-state.<br>For details of pull-up/pull-down controls of P0[7:0], Please see to the Power Management section(8.15). | R/W | Unknown |

### 8.2.2. Port Direction Registers(SFR area)

**PORT-0 OUTPUT ENABLE REGISTER (P0OEN, 0xB1)**

This register is SFR for setting the PORT-0 directions.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | P0OEN[7:0] | When writing a '1' to the port direction SFR bit, sets the corresponding bit to be an input.<br>Writing a '0' causes the port bit to be an output. | R/W | 0xFF |

**PORT-1 OUTPUT ENABLE REGISTER (P1OEN, 0xB2)**

This register is SFR for setting the PORT-1 directions.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | P1OEN[7:0] | When writing a '1' to the port direction SFR bit, sets the corresponding bit to be an input.<br>Writing a '0' causes the port bit to be an output.<br>*Note: The P1OEN[2] and P1OEN[5] are reserved bits. | R/W | 0xFF |

**PORT-3 OUTPUT DATA REGISTER (P3OEN, 0xB4)**

This register is SFR for setting the PORT-3 directions.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | P3OEN[7:0] | When writing a '1' to the port direction SFR bit, sets the corresponding bit to be an input.<br>Writing a '0' causes the port bit to be an output. | R/W | 0xFF |

### 8.2.3. Port Input Enable Registers (SFR area)

**PORT-0 INPUT ENABLE REGISTER (P0_IE, 0xB9)**

This register is SFR for enabling or disabling the inputs from the external PORT-0 PADs.
Please refer to [Figure 10] and [Table 6] above for PAD IN/OUT pins and operation modes.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | P0_IE[7:0] | When writing a '1' to the PORT-0 PAD input enable SFR bit, enabled the input from the corresponding PORT-0 PAD.<br>Writing a '0' causes the input from PAD to be disabled. | R/W | 0xFF |

**PORT-1 INPUT ENABLE REGISTER (P1_IE, 0xBA)**

This register is SFR for enabling or disabling the inputs from the external PORT-1 PADs.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | P1_IE[7:0] | When writing a '1' to the PORT-1 PAD input enable SFR bit, enabled the input from the corresponding PORT-1 PAD.<br>Writing a '0' causes the input from PAD to be disabled.<br>● *Note: The P1_IE[2] and P1_IE[5] are reserved bits. | R/W | 0xFF |

**PORT-3 INPUT ENABLE REGISTER (P3_IE, 0xBC)**

This register is SFR for enabling or disabling the inputs from the external PORT-3 PADs.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | P3_IE[7:0] | When writing a '1' to the PORT-3 PAD input enable SFR bit, enabled the input from the corresponding PORT-3 PAD.<br>Writing a '0' causes the input from PAD to be disabled. | R/W | 0xFF |

## 8.2.4. Port Drive Strength Selection Registers (SFR area)

**PORT-0 DRIVE STRENGTH SELECTION REGISTER (P0_DS, 0xC1)**

This register is SFR for selecting the drive strength capability of PORT-0.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | P0_DS[7] | Select the drive strength of P0[7]-pin<br>(0 : 4 mA , 1: 8 mA) | R/W | 0 |
| 6 | P0_DS[6] | Select the drive strength of P0[6]-pin<br>(0 : 4 mA , 1: 8 mA) | R/W | 0 |
| 5 | P0_DS[5] | Select the drive strength of P0[5]-pin<br>(0 : 4 mA , 1: 8 mA) | R/W | 0 |
| 4 | P0_DS[4] | Select the drive strength of P0[4]-pin<br>(0 : 12 mA , 1: 16 mA) | R/W | 0 |
| 3 | P0_DS[3] | Select the drive strength of P0[3]-pin<br>(0 : 12 mA , 1: 16 mA) | R/W | 0 |
| 2 | P0_DS[2] | Select the drive strength of P0[2]-pin<br>(0 : 12 mA , 1: 16 mA) | R/W | 0 |
| 1 | P0_DS[1] | Select the drive strength of P0[1]-pin<br>(0 : 12 mA , 1: 16 mA) | R/W | 0 |
| 0 | P0_DS[0] | Select the drive strength of P0[0]-pin<br>(0 : 12 mA , 1: 16 mA) | R/W | 0 |

**PORT-1 DRIVE STRENGTH SELECTION REGISTER (P1_DS, 0xC2)**

This register is SFR for selecting the drive strength capability of PORT-1.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | P1_DS[7] | Select the drive strength of P1[7]-pin<br>(0 : 4 mA , 1: 8 mA) | R/W | 0 |
| 6 | P1_DS[6] | Select the drive strength of P1[6]-pin<br>(0 : 4 mA , 1: 8 mA) | R/W | 0 |
| 5 | | Reserved bit | RO | 0 |
| 4 | P1_DS[4] | Select the drive strength of P1[4]-pin<br>(0 : 4 mA , 1: 8 mA) | R/W | 0 |
| 3 | P1_DS[3] | Select the drive strength of P1[3]-pin<br>(0 : 4 mA , 1: 8 mA) | R/W | 0 |
| 2 | | Reserved bit | RO | 0 |
| 1 | P1_DS[1] | Select the drive strength of P0[1]-pin<br>(0 : 4 mA , 1: 8 mA) | R/W | 0 |
| 0 | P1_DS[0] | Select the drive strength of P0[0]-pin<br>(0 : 4 mA , 1: 8 mA) | R/W | 0 |

**PORT-3 DRIVE STRENGTH SELECTION REGISTER (P3_DS, 0xC4)**

This register is SFR for selecting the drive strength capability of PORT-3.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | P3_DS[7] | Select the drive strength of P3[7]-pin<br>(0 : 4 mA , 1: 8 mA) | R/W | 0 |
| 6 | P3_DS[6] | Select the drive strength of P3[6]-pin<br>(0 : 4 mA , 1: 8 mA) | R/W | 0 |
| 5 | P3_DS[5] | Select the drive strength of P3[5]-pin<br>(0 : 4 mA , 1: 8 mA) | R/W | 0 |
| 4 | P3_DS[4] | Select the drive strength of P3[4]-pin<br>(0 : 4 mA , 1: 8 mA) | R/W | 0 |
| 3 | P3_DS[3] | Select the drive strength of P3[3]-pin<br>(0 : 4 mA , 1: 8 mA) | R/W | 0 |
| 2 | P3_DS[2] | Select the drive strength of P3[2]-pin<br>(0 : 4 mA , 1: 8 mA) | R/W | 0 |
| 1 | P3_DS[1] | Select the drive strength of P3[1]-pin<br>(0 : 4 mA , 1: 8 mA) | R/W | 0 |
| 0 | P3_DS[0] | Select the drive strength of P3[0]-pin<br>(0 : 4 mA , 1: 8 mA) | R/W | 0 |

### 8.2.5. Port Pull-up/down Control Registers

These registers are mapped to the DATA memory area and can be accessed by MOVX instruction of 8051 core. These registers value are retained in the power down mode.
Please refer to the GPIOPS0/GPIOPE0, GPIOPS1/GPIOPE1, GPIOPS3/GPIOPE3 registers in the section 8.21 for details on the register setting.

### 8.2.6. Port Interrupt Control Registers (SFR area)

The interrupt generation from GPIO pins is valid only under the normal mode. In the power down mode, all GPIO pins can be only used as the wakeup sources depending on the always-on register setting. (Please refer to the Sec 8.21.)
The interrupt vector address is also different in case of normal mode and power down mode. ( normal: 0x83, power down:0x7B)

**PORT-0 INTERRUPT POLARITY SELECTION REGISTER (P0_POL, 0xEA)**

This register is SFR for selecting the active interrupt polarity of PORT-0.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | P0_POL[7] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |
| 6 | P0_POL[6] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |
| 5 | P0_POL[5] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |
| 4 | P0_POL[4] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |
| 3 | P0_POL[3] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |
| 2 | P0_POL[2] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |
| 1 | P0_POL[1] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |
| 0 | P0_POL[0] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |

**PORT-0 INTERRUPT EDGE SELECTION REGISTER (P0_EDGE, 0xEB)**

This register is SFR for selecting the interrupt mode of PORT-0.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | P0_EDGE[7] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |
| 6 | P0_EDGE[6] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |
| 5 | P0_EDGE[5] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |
| 4 | P0_EDGE[4] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |
| 3 | P0_EDGE[3] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |
| 2 | P0_EDGE[2] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |
| 1 | P0_EDGE[1] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |
| 0 | P0_EDGE[0] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |

**PORT-0 INTERRUPT ENABLE REGISTER (P0_IRQ_EN, 0xEC)**

This register is SFR for selecting the interrupt enabled/disabled function of PORT-0.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | P0_IRQ_EN[7] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |
| 6 | P0_IRQ_EN[6] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |
| 5 | P0_IRQ_EN[5] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |
| 4 | P0_IRQ_EN[4] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |
| 3 | P0_IRQ_EN[3] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |
| 2 | P0_IRQ_EN[2] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |
| 1 | P0_IRQ_EN[1] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |
| 0 | P0_IRQ_EN[0] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |

**PORT-0 INTERRUPT FLAG REGISTER (P0_IRQ_STS, 0xED)**

This register is SFR for reflecting the interrupt status flags of PORT-0.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | P0_IRQ_STS[7] | 0 : No interrupt generation for P0[7]<br>1 : the pending interrupt generation for P0[7]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |
| 6 | P0_IRQ_STS[6] | 0 : No interrupt generation for P0[6]<br>1 : the pending interrupt generation for P0[6]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |
| 5 | P0_IRQ_STS[5] | 0 : No interrupt generation for P0[5]<br>1 : the pending interrupt generation for P0[5]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |

| | | | | |
|---|---|---|---|---|
| 4 | P0_IRQ_STS[4] | 0 : No interrupt generation for P0[4]<br>1 : the pending interrupt generation for P0[4]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |
| 3 | P0_IRQ_STS[3] | 0 : No interrupt generation for P0[3]<br>1 : the pending interrupt generation for P0[3]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |
| 2 | P0_IRQ_STS[2] | 0 : No interrupt generation for P0[2]<br>1 : the pending interrupt generation for P0[2]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |
| 1 | P0_IRQ_STS[1] | 0 : No interrupt generation for P0[1]<br>1 : the pending interrupt generation for P0[1]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |
| 0 | P0_IRQ_STS[0] | 0 : No interrupt generation for P0[0]<br>1 : the pending interrupt generation for P0[0]<br>● *Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |

**PORT-1 INTERRUPT POLARITY SELECTION REGISTER (P1_POL, 0xF2)**

This register is SFR for selecting the active interrupt polarity of PORT-1.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | P1_POL[7] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |
| 6 | P1_POL[6] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |
| 5 | | Reserved bit | RO | 0 |
| 4 | P1_POL[4] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |
| 3 | P1_POL[3] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |
| 2 | | Reserved bit | RO | 0 |
| 1 | P1_POL[1] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |
| 0 | P1_POL[0] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |

**PORT-1 INTERRUPT EDGE SELECTION REGISTER (P1_EDGE, 0xF3)**

This register is SFR for selecting the interrupt mode of PORT-1.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | P1_EDGE[7] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |
| 6 | P1_EDGE[6] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |
| 5 | | Reserved bit | RO | 0 |
| 4 | P1_EDGE[4] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |
| 3 | P1_EDGE[3] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |
| 2 | | Reserved bit | RO | 0 |
| 1 | P1_EDGE[1] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |
| 0 | P1_EDGE[0] | 0 : level interrupt mode | R/W | 0 |

| | | | | |
|---|---|---|---|---|
| | | 1 : edge interrupt mode | | |

**PORT-1 INTERRUPT ENABLE REGISTER (P1_IRQ_EN, 0xF4)**

This register is SFR for selecting the interrupt enabled/disabled function of PORT-1.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | P1_IRQ_EN[7] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |
| 6 | P1_IRQ_EN[6] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |
| 5 | | Reserved bit | RO | 0 |
| 4 | P1_IRQ_EN[4] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |
| 3 | P1_IRQ_EN[3] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |
| 2 | | Reserved bit | RO | 0 |
| 1 | P1_IRQ_EN[1] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |
| 0 | P1_IRQ_EN[0] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |

**PORT-1 INTERRUPT FLAG REGISTER (P1_IRQ_STS, 0xF5)**

This register is SFR for reflecting the interrupt status flags of PORT-1.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | P1_IRQ_STS[7] | 0 : No interrupt generation for P1[7]<br>1 : the pending interrupt generation for P1[7]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |
| 6 | P1_IRQ_STS[6] | 0 : No interrupt generation for P1[6]<br>1 : the pending interrupt generation for P1[6]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |
| 5 | | Reserved bit | RO | 0 |
| 4 | P1_IRQ_STS[4] | 0 : No interrupt generation for P1[4]<br>1 : the pending interrupt generation for P1[4]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |
| 3 | P1_IRQ_STS[3] | 0 : No interrupt generation for P1[3]<br>1 : the pending interrupt generation for P1[3]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |
| 2 | | Reserved bit | RO | 0 |
| 1 | P1_IRQ_STS[1] | 0 : No interrupt generation for P1[1]<br>1 : the pending interrupt generation for P1[1]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |
| 0 | P1_IRQ_STS[0] | 0 : No interrupt generation for P1[0]<br>1 : the pending interrupt generation for P1[0]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |

**PORT-3 INTERRUPT POLARITY SELECTION REGISTER (P3_POL, 0xFA)**

This register is SFR for selecting the active interrupt polarity of PORT-3.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | P3_POL[7] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |
| 6 | P3_POL[6] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |
| 5 | P3_POL[5] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |
| 4 | P3_POL[4] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |
| 3 | | Reserved bit | RO | 0 |
| 2 | | Reserved bit | RO | 0 |
| 1 | P3_POL[1] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |
| 0 | P3_POL[0] | 0 : low level/falling edge interrupt selection<br>1 : high level/rising edge interrupt selection | R/W | 0 |

**PORT-3 INTERRUPT EDGE SELECTION REGISTER (P3_EDGE, 0xFB)**

This register is SFR for selecting the interrupt mode of PORT-3.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | P3_EDGE[7] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |
| 6 | P3_EDGE[6] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |
| 5 | P3_EDGE[5] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |
| 4 | P3_EDGE[4] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |
| 3 | | Reserved bit | RO | 0 |
| 2 | | Reserved bit | RO | 0 |
| 1 | P3_EDGE[1] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |
| 0 | P3_EDGE[0] | 0 : level interrupt mode<br>1 : edge interrupt mode | R/W | 0 |

**PORT-3 INTERRUPT ENABLE REGISTER (P3_IRQ_EN, 0xFC)**

This register is SFR for selecting the interrupt enabled/disabled function of PORT-3.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | P3_IRQ_EN[7] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |
| 6 | P3_IRQ_EN[6] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |
| 5 | P3_IRQ_EN[5] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |
| 4 | P3_IRQ_EN[4] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |
| 3 | | Reserved bit | RO | 0 |
| 2 | | Reserved bit | RO | 0 |
| 1 | P3_IRQ_EN[1] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |
| 0 | P3_IRQ_EN[0] | 0: interrupt generation disabled<br>1: interrupt generation enabled | R/W | 0 |

**PORT-3 INTERRUPT FLAG REGISTER (P3_IRQ_STS, 0xFD)**

This register is SFR for reflecting the interrupt status flags of PORT-3.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | P3_IRQ_STS[7] | 0 : No interrupt generation for P3[7]<br>1 : the pending interrupt generation for P3[7]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |
| 6 | P3_IRQ_STS[6] | 0 : No interrupt generation for P3[6]<br>1 : the pending interrupt generation for P3[6]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |
| 5 | P3_IRQ_STS[5] | 0 : No interrupt generation for P3[5]<br>1 : the pending interrupt generation for P3[5]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |
| 4 | P3_IRQ_STS[4] | 0 : No interrupt generation for P3[4]<br>1 : the pending interrupt generation for P3[4]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |
| 3 | | Reserved bit | RO | 0 |
| 2 | | Reserved bit | RO | 0 |
| 1 | P3_IRQ_STS[1] | 0 : No interrupt generation for P3[1]<br>1 : the pending interrupt generation for P3[1]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |
| 0 | P3_IRQ_STS[0] | 0 : No interrupt generation for P3[0]<br>1 : the pending interrupt generation for P3[0]<br>*Note: For the interrupt clear, the 1 must be written to this bit. | R/W | 0 |

**PORTs INTERRUPT PENDING REGISTER (GPIO_IRQ_PEND, 0xF1)**

This register is SFR for reflecting the pending interrupt flags of PORT-0/1/3.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:3 | | Reserved bits | RO | 0 |
| 2 | P3_IRQ_PEND | 0 : No interrupt generation<br>1 : The pending interrupt flag for Port-3 | RO | 0 |
| 1 | P1_IRQ_PEND | 0 : No interrupt generation<br>1 : The pending interrupt flag for Port-1 | RO | 0 |
| 0 | P0_IRQ_PEND | 0 : No interrupt generation<br>1 : The pending interrupt flag for Port-0 | RO | 0 |

## 8.3. TIMER 0/1

The Embedded MCU has two 16-bit timers which are compatible with Intel 8051 MCU (Timer0, Timer1). These timers have 2 modes; one is operated as a timer and the other is operated as a counter. When it is operated as a timer, there are 4 operating modes.
Each timer is 16-bit timer and consists of two 8-bit register. Therefore, the counter can be either 8-bit or 16-bit set by the operating mode.
In counter mode, the input signal T0 (P3 [4]) and T1 (P3 [5]) are sampled once every 12 cycles of the system clock. If the sampled value is changed from '1' to '0', the internal counter is incremented. In this time, the duty cycle of T0 and T1 doesn't affect the increment.
Timer0 and Timer1 are accessed by using 6 SFR's.
The following table describes timer registers and modes.

**TCON (TIMER/COUNTER CONTROL REGISTER,0x88)**
This register is used to control a timer function and monitor a timer status.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | TF1 | Timer1 Overflow Flag.<br>When this field is '1', a Timer1 interrupt occurs. After the Timer1 interrupt service routine is executed, this field value is cleared by hardware. | R/W | 0 |
| 6 | TR1 | Timer1 Run Control.<br>When this bit is set to '1', Timer1 is enabled. | R/W | 0 |
| 5 | TF0 | Timer0 Interrupt Flag.<br>1: Interrupt is pending<br>After Timer0 interrupt service routine is executed, this field is cleared by hardware. | R/W | 0 |
| 4 | TR0 | Timer0 Run<br>When this bit is set to '1', Timer0 is enabled. | R/W | 0 |
| 3 | IE1 | External Interrupt1 Edge Flag.<br>When this field is '1', External interrupt1 is pending. After the interrupt service routine is executed, this field is cleared by hardware. | R/W | 0 |
| 2 | IT1 | External Interrupt1 Type Control.<br>This field specifies the type of External interrupt1.<br>1=Edge type. When the falling edge of INT1 is detected, the interrupt occurs.<br>0=Level type. When INT1 is low level, the interrupt occurs. | R/W | 0 |
| 1 | IE0 | External Interrupt0 Edge Flag.<br>When this field is '1', External interrupt0 is pending. After the interrupt service routine is executed, this field is cleared by hardware. | R/W | 0 |
| 0 | IT0 | External Interrupt0 Type Control.<br>This field specifies the type of External interrupt0.<br>1=Edge type. When the falling edge of INT0 is detected, the interrupt occurs.<br>0=Level type. When INT0 is low level, the interrupt occurs. | R/W | 0 |

**TMOD (TIMER/COUNTER MODE CONTROL REGISTER, 0x89)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | GATE 1 | Timer Gate Control<br>When TR1 is set to '1' and GATE1 is '1', Timer1 is enabled only while INT1 pin is high. When GATE1 is set to '0', Timer1 is enabled whenever TR1 control is set to '1'. | R/W | 0 |
| 6 | CT1 | Timer1 Counter Mode Select<br>When this field is set to '1', Timer1 is enabled as counter mode. | R/W | 0 |
| 5:4 | M1 | Timer1 mode select.<br>0: Mode0, 12-bit Timer<br>1: Mode1, 16-bit Timer<br>2: Mode2, 8-bit Timer with auto-load<br>3: Mode3, two 8-bit Timer | R/W | 0 |
| 3 | GATE 0 | Timer0 Gate Control.<br>When TR0 is set to '1' and GATE0 is '1', Timer0 is enabled while INT0 pin is in high.<br>When GATE1 is set to '0' and TR1 is set to '1', Timer0 is enabled. | R/W | 0 |
| 2 | CT0 | When this field is set to '1', Timer0 is enabled as counter mode. | R/W | 0 |
| 1:0 | M0 | Timer0 mode select<br>0: Mode0, 12-bit Timer<br>1: Mode1, 16-bit Timer<br>2: Mode2, 8-bit Timer with auto-load<br>3: Mode3, two 8-bit Timer | R/W | 0 |

**TL0/TL1/TH0/TH1 (TIMER REGISTERS, 0x8A, 0x8B, 0x8C, 0x8D)**

A pair of register, which are (TH0, TL0) and (TH1, TL1), can be used as 16-bit timer register for Timer0 and Timer1 and it can be used as 8-bit register respectively.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | TH1 | Timer1 High Byte Data | R/W | 0x00 |

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | TH0 | Timer0 High Byte Data | R/W | 0x00 |

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | TL1 | Timer1 Low Byte Data | R/W | 0x00 |

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | TL0 | Timer0 Low Byte Data | R/W | 0x00 |

In mode0, 13-bit register of timer0 consists of all 8-bits of TH0 and the lower 5-bits of TL0. The upper 3-bit of TL0 are disregarded. When this 13-bit register is overflowed, set TF0 to '1'. The operation of timer1 is same as that of timer0.

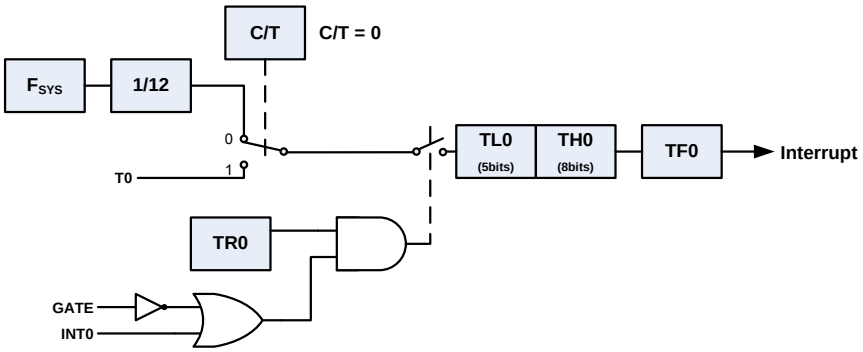



**Figure 11. Timer0 Mode0**

In Mode1, the operation is same as it of Mode0 except all timer registers are enabled as a 16-bit counter.

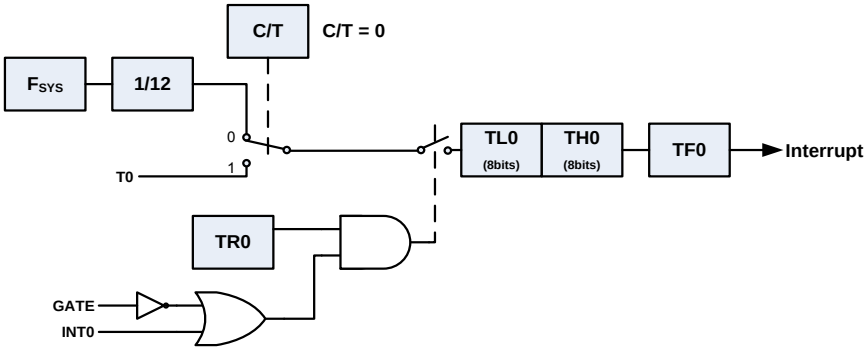



**Figure 12. Timer0 Mode1**

In mode2, TL0 of Timer0 is enabled as an 8-bit counter and TH0 reloads TL0 automatically. TF0 is set to '1' by overflowing of TL0. TH0 value retains the previous value regardless of the reloading. The operation of Timer1 is same as that of Timer0.

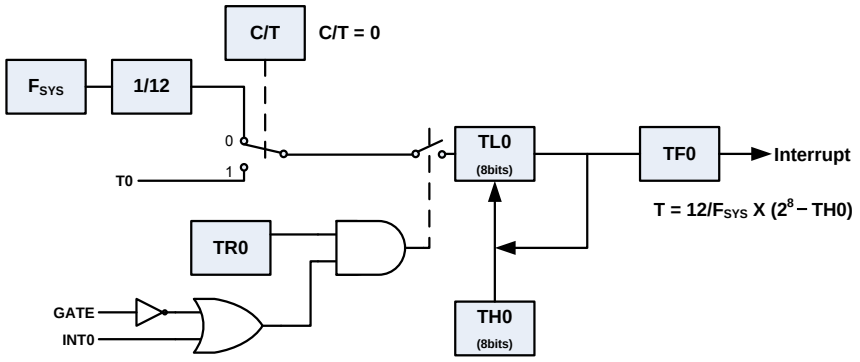



**Figure 13. Timer0 Mode2**

In Mode3, Timer0 uses TL0 and TH0 as an 8-bit timer respectively. In other words, it uses two counters. TL0 controls as the control signals of Timer0. TH0 is always used as a timer function and it controls as TR1 of Timer1. The overflow is stored in TF1. At this time, Timer1 is disabled and it retains the previous value.

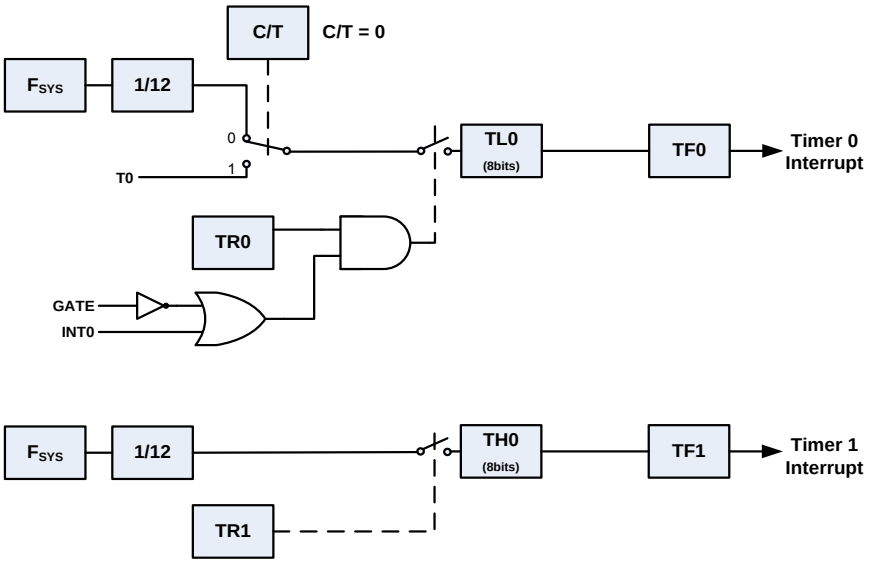



**Figure 14. Timer0 Mode3**

## 8.4. TIMER 2/3

The embedded MCU includes two 16-bit timers (Timer2 and Timer3).

**T23CON (TIMER2/3 CONTROL REGISTER, 0xA9)**

This register is used to control Timer2 and Time3.

<table>
<tr><th>Bit Field</th><th>Name</th><th>Descriptions</th><th>R/W</th><th>Reset Value</th></tr>
<tr><td>7</td><td>T3_DIV2</td><td rowspan="3">Timer3 clock division ratio selection<br><table><tr><th>Bit values</th><th>Clock ratio</th></tr><tr><td>3’b000</td><td>Divided by 1</td></tr><tr><td>3’b001</td><td>Divided by 2</td></tr><tr><td>3’b010</td><td>Divided by 3 (default value)</td></tr><tr><td>3’b011</td><td>Divided by 4</td></tr><tr><td>3’b100</td><td>Divided by 8</td></tr><tr><td>3’b101</td><td>Divided by 16</td></tr><tr><td>3’b110</td><td>Divided by 32</td></tr><tr><td>3’b111</td><td>Divided by 64</td></tr></table></td><td>R/W</td><td>0</td></tr>
<tr><td>6</td><td>T3_DIV1</td><td>R/W</td><td>1</td></tr>
<tr><td>5</td><td>T3_DIV0</td><td>R/W</td><td>0</td></tr>
<tr><td>4</td><td>TR3</td><td>Timer3 Run.<br>When this field is set to ‘1’, Timer3 is operated.</td><td>R/W</td><td>0</td></tr>
<tr><td>3</td><td>T2_DIV2</td><td rowspan="3">Timer2 clock division ratio selection<br><table><tr><th>Bit values</th><th>Clock ratio</th></tr><tr><td>3’b000</td><td>Divided by 1</td></tr><tr><td>3’b001</td><td>Divided by 2</td></tr><tr><td>3’b010</td><td>Divided by 4</td></tr><tr><td>3’b011</td><td>Divided by 8 (default value)</td></tr><tr><td>3’b100</td><td>Divided by 16</td></tr><tr><td>3’b101</td><td>Divided by 32</td></tr><tr><td>3’b110</td><td>Divided by 64</td></tr><tr><td>3’b111</td><td>Divided by 8</td></tr></table></td><td>R/W</td><td>0</td></tr>
<tr><td>2</td><td>T2_DIV1</td><td>R/W</td><td>1</td></tr>
<tr><td>1</td><td>T2_DIV0</td><td>R/W</td><td>1</td></tr>
<tr><td>0</td><td>TR2</td><td>Timer2 Run.<br>When this field is set to ‘1’, Timer2 is operated.</td><td>R/W</td><td>0</td></tr>
</table>

**TL2/TL3/TH2/TH3 (TIMER2/3 TIMER REGISTER, 0xAC, 0xAD, 0xAA, 0xAB)**
Register (TH2, TL2) and (TH3, TL3) are 16-bit timer counter register for Timer2 and Timer3. The maximum allowed set value is 0xFFFE.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | TL3 | Timer3 Low Byte Data | R/W | 0x00 |

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | TL2 | Timer2 Low Byte Data | R/W | 0x00 |

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | TH3 | Timer3 High Byte Data | R/W | 0x00 |

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | TH2 | Timer2 High Byte Data | R/W | 0x00 |

Timer2 acts as a general 16-bit timer. Time-out period is calculated by the following equation;

$$T_2 = \frac{T23CON[3:1]division \times (256 \times TH2 + TL2 + 1)}{fsystem}$$

If the time-out period is set too short, excessive interrupt causing abnormal operation of the system will occur. It is recommended to set sufficient time-out period for Timer2 (over 100μs).

Timer3 acts as a general 16-bit timer. Time-out period of Timer3 is calculated by the following equation;

$$T_3 = \frac{T23CON[7:4]division \times (256 \times TH3 + TL3 + 1)}{fsystem}$$

If the time-out period is set too short, excessive interrupt causing abnormal operation of the system will occur. It is recommended to set Timer3 to a sufficient time-out period.

## 8.5. PWMs

The PWM is a user-programmable PWM and can also supports timer and counter controller features. Its use is to implement functions like Pulse Width Modulation (PWM), timer and counter facilities.

The following lists the main features of PWM core.

- 5 channel support
- 16-bit counter/timer facility
- Single-run or continues run of PTC counter
- Programmable PWM mode
- HI/LO Reference and Capture registers
- PWM/Timer/Counter functionalities can cause an interrupt to the CPU

$$T = \frac{CNTR}{f_{system}}$$

When operating in PWM mode, the PWM core generates binary signal with user programmable low and high periods.

When operating in timer/counter mode, the PWM core counts number of clock cycles of system clock. After reaching low and/or high reference, the PWM core can generate an interrupt. Input signal PWM pad can be used to capture value of the CNTR register into low and high capture registers.

When operating from the system clock, PTC_GATE pin can be used to gate internal timer/counter circuitry. In both PWM and timer/counter modes, CNTR can run for a single cycle and it can automatically restart after each complete cycle. Cycle completes after reaching value in the LRC register. These two modes are called single-run and continuous-run.

**PWM Mode**
To operate in PWM mode, HRC and LRC should be set with the value of low and high periods of the PWM output signal. HRC is number of clock cycles after reset of the CNTR when PWM output should go high. And LRC is number of clock cycles after reset of the CNTR when PWM output should go low.
CNTR can be reset with the hardware reset, bit CTRL[CNTRRST] or periodically when CTRL[SINGLE] bit is cleared. To enable PWM output driver, CTRL[OE] should be set. To enable continues operation, CTRL[SINGLE] should be cleared and CTRL[EN] should be set. If gate function is enabled, PWM periods can be automatically adjusted with the capture input. PWM output signal is controlled with the HRC and LRC, and these two registers can be set without software control with the PTC_GATE pin signal.

Usually interrupts are enabled in timer/counter mode. This is done with the CTRL[INTE].

**Gate Feature**
If system clock is used to increment CNTR, PTC_GATE pin input signal can be used to gate the system clock and not increment the CNTR register. Which level of the PTC_GATE pin has gating capability depends on value of the CTRL[NEC].

**Interrupt Feature**
Whenever CNTR equals to the value of the HRC or LRC, an interrupt request can be asserted. This depends if CTRL[INTE] bit is set.

**Capture Feature**
PWM pin input signal can be used to capture value of the current CNTR into HRC or LRC registers. Into which reference/capture register value is captured, depends on edge of the PWM pin input signal. On positive edge value is captured into HRC register and on negative edge value is captured into LRC register. In order to enable capture feature, CTRL[CAPTE] must be set.

**PWMx_CNTR**
CNTR register is the actual counter register. It is incremented at every counter/timer clock cycle. In order to count, CNTR must first be enabled with the CTRL[EN]. CNTR can be reset with the CTRL[RST]. CNTR can operate in either single-run mode or continues mode. Mode is selected with the CTRL[SINGLE].

**PWMx_CNTRH(PWM CHx COUNTER REGISTER MSB PART, 0x2580(CH0), 0x2588(CH1), 0x2590(CH2), 0x2598(CH3), 0x25A0(CH4))**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 15:8 | CNTR | MSB Part of CNTR register | R/W | 0 |

**PWMx_CNTRL(PWM CHx COUNTER REGISTER LSB PART, 0x2581(CH0), 0x2589(CH1), 0x2591(CH2), 0x2599(CH3), 0x25A1(CH4))**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | CNTR | LSB Part of CNTR register | R/W | 0 |

**PWMx_HRC**

HRC register is a second out of two reference/capture registers. It has two functions;

- In reference mode it is used to assert high PWM output or to generate an interrupt.
- In capture mode it captures CNTR value on high value of PWM pin input signal.

The HRC should have lower value than LRC. This is because PWM output goes first high and later low.

**PWMx_HRCH (PWM CHx HIGH REF/CAP REGISTER, MSB Part, 0x2582(CH0), 0x258A(CH1), 0x2592(CH2), 0x259A(CH3), 0x25A2(CH4))**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 15:8 | HRC | MSB Part of HRC register | R/W | 0 |

**PWMx_HRCL (PWM CH0 HIGH REF/CAP REGISTER, LSB Part, 0x2583(CH0), 0x258B(CH1), 0x2593(CH2), 0x259B(CH3), 0x25A3(CH4))**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | HRC | LSB Part of HRC register | R/W | 0 |

**PWMx_LRC**

LRC register is a first out of two reference/capture registers. It has two functions;

□□- In reference mode it is used to assert low PWM output or to generate an interrupt
□□- In capture mode it captures CNTR value on low value of PWM pin input signal

The LRC should have higher value than HRC. This is because PWM output goes high first and then low later.

**PWMx_LRCH (PWM CHx LOW REF/CAP REGISTER, MSB Part, 0x2584(CH0), 0x258C(CH1), 0x2594(CH2), 0x259C(CH3), 0x25A4(CH4))**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 15:8 | LRC | MSB Part of LRC register | R/W | 0 |

**PWMx_LRCL (PWM CHx LOW REF/CAP REGISTER, LSB Part, 0x2585(CH0), 0x258D(CH1), 0x2595(CH2), 0x259D(CH3), 0x25A5(CH4))**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | LRC | LSB Part of LRC register | R/W | 0 |

**PWMx_CTRL**
Control bits in CTRL register control operation of PWM core.

**PWMx_CTRL (PWM CHx CONTROL REGISTER, 0x2586(CH0), 0x258E(CH1), 0x2596(CH2), 0x259E(CH3), 0x25A6(CH4))**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | INTE | Interrupt Enable | R/W | 0 |
| 6 | CAPTE | When set, PWM pin input signal can be used to capture CNTR into LRC or HRC registers. Into which reference/capture register capture occurs depends on edge of the PWM pin input signal. When cleared, capture function is masked. | R/W | 0 |
| 5 | CNTRRST | When set, CNTR is under reset.<br>When cleared, normal operation of the counter is allowed. | R/W | 0 |
| 4 | SINGLE | When set, CNTR is not incremented anymore after it reaches value equal to the LRC value. When cleared, CNTR is restarted after it reaches value in the LCR register. | R/W | 0 |
| 3 | OE | The value of this bit is reflected on the PWM pin output signal. It is used to enable PWM output driver. | R/W | 0 |
| 2 | NEC | When set, CNTR increments on low period of PTC_GATEx pin.<br>When cleared, CNTR increments on high period of PTC_GATEx pin.<br>This bit has effect only on 'gating' function of PTC_GATEx pin when GATE bit is set. | R/W | 0 |
| 1 | GATE | PTC_GATEx pin gate function enable<br>When set, the PTC_GATEx pin is used to increase the internal 16-bit counter /timer(CNTR). | R/W | 0 |
| 0 | EN | When set, CNTR can be incremented. | R/W | 0 |

**PWM_INTR (PWM INTERRUT FLAG REGISTER, 0x257F)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:5 | Reserved | - | RO | 0 |
| 4 | PWM4INTR | PWM CH4 Interrupt flag. | R/W | 0 |
| 3 | PWM3INTR | PWM CH3 Interrupt flag. | R/W | 0 |
| 2 | PWM2INTR | PWM CH2 Interrupt flag. | R/W | 0 |
| 1 | PWM1INTR | PWM CH1 Interrupt flag. | R/W | 0 |
| 0 | PWM0INTR | PWM CH0 Interrupt flag. | R/W | 0 |

## 8.6. Watchdog Timer

Watchdog Timer (WDT) monitors whether the MCU operates normally or not. If a problem occurs, it immediately resets MCU.

In fact, when a system does not clear WDT counter value, WDT considers that a problem occurred. Therefore, it automatically resets MCU. WDT is used when a program is not completed normally because a software error is caused in any environment such as electrical noise, unstable power, and static electricity.

When Power-up, the internal counter value of WDT is set to '0' and watchdog timer is operated. If overflow is caused in the internal counter, system reset is caused. At this moment, timeout period is about 1.0 second. A user may not use WDT by setting ENB bit of WDTCON register. When WDT operates, an application program must clear CLR bit periodically to prevent a system from being reset.

The overflow interval can be set by DUR bits. The interval calculated as follows;

$$T = \frac{2^{DUR}}{fRTCCLK}$$

To protect WDTCON register write access, special write sequence is required.

WDTCON ← 0x55 (write password 1)
WDTCON ← 0xAA (write password 2)
WDTCON ← (Control Value)

If the special sequence is not applied, it immediately resets MCU.

**WDTCON (WATCHDOG TIMER CONTROL REGISTER, MCU SFR 0xD2)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | ENB | Watchdog Timer Enable Bar. Active Low | R/W | 0 |
| 6 | CLR | Watchdog Timer Clear. Auto Clear Bit. This bit clear Internal WDT Counter. | WO | 0 |
| 5 | SYNCBUSY | Synch Busy. This bit indicates during WDT register update. | R/W | 0 |
| 3:0 | DUR | Watchdog Timer Duration | R/W | 0xF |

## 8.7. UART 0/1

Serial communication is categorized as synchronous mode or asynchronous mode in terms of its data transmission method. Synchronous mode is to transmit the data based on the standard clock pulse. Asynchronous mode is to transmit the data bit by arranging the baud rate of data bit each other without standard clock. That is, when a transmitter transmits the data as arranged frequency, a receiver read the data according to the arranged method previously.

The embedded MCU has UART0 and UART1 to enable two-way communication.
These devices support asynchronous mode. The following registers are used to control UART. The baudrate can be set by following expression;

$$Baudrate = \frac{fsystem}{XCR \times Divisor(16bits)}$$

**RBR (UART0 RECEIVE BUFFER REGISTER, 0x2500)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | RBR | Read the received data | RO | 0x00 |

**THR (UART0 TRANSMITTER HOLDING REGISTER, 0x2500)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | THR | This register stores the data to be transmitted. The address is the same as RBR register. When accessing this address, received data(RBR) is read and the data to be transmitted is stored. | WO | 0x00 |

**DLL (UART0 DIVISOR LSB REGISTER, 0x2500)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | DLL | This register can be accessed only when DLAB bit in the LCR register is set to '1'. This register shares a 16-bit register with the DLM register occupying the lower 8 bits. This full 16-bit register is used to divide clock. | R/W | 0x00 |

**IER (UART0 INTERRUPT ENABLE REGISTER, 0x2501)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:4 | | Reserved | RO | 0 |
| 3 | EDSSI | Enable MODEM Status Interrupt.<br>When this field is set to '1', Modem status interrupt is enabled. | R/W | 0 |
| 2 | ELSI | Enable Receiver Line Status Interrupt. | R/W | 0 |
| 1 | ETBEI | Enable Transmitter Holding Register Empty Interrupt | R/W | 0 |
| 0 | ERBEI | Enable Received Data Available Interrupt | R/W | 0 |

**DLM (UART0 DIVISOR LATCH MSB REGISTER, 0x2501)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | DLM | This register can be accessed only when DLAB bit in the LCR register is set to '1'. This register shares a 16-bit register with the DLL register occupying the higher 8 bits. This full 16-bit register is used to divide clock. | R/W | 0x00 |

**IIR (UART0 INTERRUPT IDENTIFICATION REGISTER, 0x2502)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:4 | | Reserved | RO | 0 |
| 3:1 | INTID | Interrupt Identification.<br>Refer to the [Table 7] below. | RO | 0 |
| 0 | PENDING | Shows whether the interrupt is pending or not. When this field is '0', the interrupt | RO | 1 |

| | | | | |
|---|---|---|---|---|
| | | is pending. | | |

*Note: IIR register uses the same address as FCR register below. IIR register is read only and FCR register is write-only.*

**Table 7. UART0 Interrupt List**

| INTID | Priority | Interrupt Type | Interrupt Source | Interrupt Reset Control |
|---|---|---|---|---|
| 011 | 1st | Receiver Line Status | Parity, Overrun or Framing errors or Break Interrupt | Reading the LSR (Line Status Register). |
| 010 | 2nd | Receiver Data available | FIFO trigger level reached | FIFO drops below trigger level |
| 110 | 2nd | Timeout Indication | There is at least 1 character in the FIFO but no character has been input to the FIFO or read from it for the last 4 character times. | Reading from the FIFO (Receiver Buffer Register) |
| 001 | 3rd | Transmitter Holding Register Empty | Transmitter Holding Register Empty | Writing to the Transmitter Holding Register or reading IIR |
| 000 | 4th | Modem Status | CTS, DSR, RI or DCD | Reading the Modem status register |

**FCR (UART0 FIFO CONTROL REGISTER, 0x2502)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:6 | URXFTRIG | Adjust the trigger level of Receiver FIFO. Interrupt occurs when FIFO receives the data byte based on this field value below. For example, when URXFTRIG field is set to '3', interrupt does not occur until FIFO receives 14 byte. When FIFO receives 14 byte, interrupt occurs.<br>0: 1byte<br>1: 4 byte<br>2: 8 byte<br>3: 14 byte | WO | 3 |
| 5:3 | | Reserved | RO | 0 |
| 2 | UTXFRST | When this field is set to '1', Transmitter FIFO is cleared and the circuits related to it are reset. | WO | 0 |
| 1 | URXFRST | When this field is set to '1', Receiver FIFO is cleared and the circuits related to it are reset. | WO | 0 |
| 0 | | Reserved | RO | 0 |

**LCR (UART0 LINE CONTROL REGISTER, 0x2503)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | DLAB | Divisor Latch Access Enable. | R/W | 0 |

| | | | | |
|---|---|---|---|---|
| | | When this field is set to '1', Divisor register (DLM, DLL) can be accessed. When this field is set to '0', general register can be accessed. | | |
| 6 | SB | Set Break.<br>When this field is set to '1', serial output is to be '0' by force(break state) | R/W | 0 |
| 5 | SP | Stick Parity.<br>When PEN and EPS is '1' while this field is set to '1', parity, which is generated as '0', is transmitted. In reception mode, it checks whether parity value is '0' or not.<br><br>When PEN is '1' and EPS is '0' while this field is set to '1', parity, which is generated as '1', is transmitted. In reception mode, it checks whether parity value is '1' or not. | R/W | 0 |
| 4 | EPS | Even Parity Enable.<br>When this field is set to '1', parity value is determined to transfer '1' which is in even number.<br>When this field is set to '0', parity value is determined to transfer '1' which is in odd number. | R/W | 0 |
| 3 | PEN | Parity Enable.<br>When this field is set to '1', parity is calculated for the byte to be transmitted and transferred with it. In reception mode, checks parity. When this field is '0', parity is not generated. | R/W | 0 |
| 2 | STB | Number of Stop Bits.<br>When this field is set to '1', 2 stop bit is used.<br>When transmitting a word (character) of 5 bit length, 1.5 stop bit is used.<br>When this field is '0', 1 stop bit is used. | R/W | 0 |
| 1:0 | WLS | Word Length Select.<br>0: 5bit Word<br>1: 6bit Word<br>2: 7bit Word<br>3: 8bit Word | R/W | 3 |

**LSR (UART0 LINE STATUS REGISTER, 0x2505)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | ERCVR | Error in Receiver Indicator.<br>1: At least one parity error, framing error or break indications have been received. The bit is cleared upon reading from the register.<br>0: Otherwise. | RO | 0 |
| 6 | TEMT | Transmitter Empty indicator.<br>1: Both the transmitter FIFO and | RO | 1 |

| | | | | |
|---|---|---|---|---|
| | | transmitter shift register are empty. The bit is cleared when data is being been written to the transmitter FIFO.<br>'0' – Otherwise. | | |
| 5 | THRE | Transmit FIFO is empty.<br>1: The transmitter FIFO is empty. Generates Transmitter Holding Register Empty interrupt. The bit is cleared when data is being been written to the transmitter FIFO.<br>0: Otherwise. | RO | 1 |
| 4 | BI | Break Interrupt (BI) indicator.<br>1: A break condition has been reached in the current character. The break occurs when the line is held in logic 0 for a time of one character (start bit + data + parity + stop bit). In that case, one zero character enters the FIFO and the UART waits for a valid start bit to receive next character. The bit is cleared upon reading from the register. Generates receiver Line Status interrupt.<br>1: No break condition in the current character. | RO | 0 |
| 3 | FE | Framing Error (FE) indicator.<br>1: The received character at the top of the FIFO did not have a valid stop bit. Of course, generally, it might be that all the following data is corrupt. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt.<br>1: No framing error in the current character. | RO | 0 |
| 2 | PE | Parity Error (PE) indicator.<br>1: The character that is currently at the top of the FIFO has been received with parity error. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt.<br>1: No parity error in the current character. | RO | 0 |
| 1 | OE | Overrun Error (OE) indicator.<br>1: If the FIFO is full and another character has been received in the receiver shift register. If another character is starting to arrive, it will overwrite the data in the shift register but the FIFO will remain intact. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt.<br>0: No overrun state | RO | 0 |
| 0 | DR | Data Ready (DR) indicator.<br>0: No characters in the FIFO.<br>1: At least one character has been received and is in the FIFO. | RO | 0 |

**XCR (UART0 DIVISOR LSB REGISTER, 0x2507)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | XCR | This register can be accessed only when DLAB bit in LCR register is set to '1'. This register consists of 8 bit register. XCR register with DLM, DLL registers used in baudrate generation. | R/W | 0x10 |

**ECR (UART0 EXTRA FEATURE CONTROL REGISTER, 0x2505)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:3 | | Reserved. | RO | 0 |
| 2:0 | ECR | Extra feature control register.<br>0: Default register access.<br>2: RX FIFO Interrupt level (RIL) register access enable.<br>5: TX FIFO level count (TLC) register and RX FIFO level count (RLC) register access enable. | WO | 0 |

**TLC (UART0 TX FIFO LEVEL COUNT REGISTER, 0x2503)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | TXLVLCNT | This register can be accessed when ECR register is set to '5'. This register indicates filled data size in the TX FIFO | RO | 0x00 |

**RIL (UART0 RX FIFO INTERRUPT LEVEL REGISTER, 0x2504)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | RXINTLVL | This register can be accessed when ECR register is set to '2'. When RIL register is set to zero value, the URXFTRIG field of FCR is valid. If RIL register is set to non-zero value, the receiver FIFO interrupt occurs when received bytes is greater than or equal to RIL register value. | R/W | 0x00 |

**RLC (UART0 RX FIFO LEVEL COUNT REGISTER, 0x2504)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | RXLVLCNT | This register can be accessed when ECR register is set to '5'. This register indicates filled data size in the RX FIFO. | RO | 0x00 |

**VSPMUX (I2S SOURCE PATH MUX CONTROL REGISTER, 0x277F)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:3 | | Reserved. | RO | 0 |
| 2:0 | VSPMUX | when VSPMUX register set to '1'. UART0 FIFO size is changed 256 entry. Otherwise, UART0 FIFO size is 16 entry. | R/W | 0 |

| | | | | |
|---|---|---|---|---|
| | | The detailed information is in the I2S Part. | | |

The following registers are to control UART1.

**RBR (UART1 RECEIVE BUFFER REGISTER, 0x2510)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | RBR | Read the received data | RO | 0x00 |

**THR (UART1 TRANSMITTER HOLDING REGISTER, 0x2510)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | THR | This register stores the data to be transmitted. The address is same as RBR register. By accessing this address, received data(RBR) can be read and the data to be transmitted can be stored. | WO | 0x00 |

**DLL (UART1 DIVISOR LSB REGISTER, 0x2510)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | DLL | This register can be accessed only when DLAB bit in LCR register is set to '1'. This register consists of 16-bit register with DLM register and it is a lower 8 bit of 16-bit. This 16-bit register is used to divide clock. | R/W | 0x00 |

**IER (UART1 INTERRUPT ENABLE REGISTER, 0x2511)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:4 | | Reserved | RO | 0 |
| 3 | EDSSI | Enable MODEM Status Interrupt.<br>When this field is set to '1', Modem status interrupt is enabled. | R/W | 0 |
| 2 | ELSI | Enable Receiver Line Status Interrupt. | R/W | 0 |
| 1 | ETBEI | Enable Transmitter Holding Register Empty Interrupt | R/W | 0 |
| 0 | ERBEI | Enable Received Data Available Interrupt | R/W | 0 |

**DLM (UART1 DIVISOR LATCH MSB REGISTER, 0x2511)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | DLM | This register can be accessed only when DLAB bit in LCR register is set to '1'. This register consists of 16-bit register with DLL register and it is a higher 8 bit of 16-bit. This 16-bit register is used to divide clock. | R/W | 0x00 |

**IIR (UART1 INTERRUPT IDENTIFICATION REGISTER, 0x2512)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:4 | | Reserved | RO | 0 |
| 3:1 | INTID | Interrupt Identification.<br>Refer to the [Table 8] below. | RO | 0 |
| 0 | PENDING | Shows whether the interrupt is pending or not. When this field is '0', the interrupt is pending. | RO | 1 |

*Note: IIR register uses the same address as FCR register below. IIR register is read only and FCR register is write-only.*

**Table 8. UART1 Interrupt List**

| INTID | Priority | Interrupt Type | Interrupt Source | Interrupt Reset Control |
|---|---|---|---|---|
| 011 | 1st | Receiver Line Status | Parity, Overrun or Framing errors or Break Interrupt | Reading the LSR (Line Status Register). |
| 010 | 2nd | Receiver Data available | FIFO trigger level reached | FIFO drops below trigger level |
| 110 | 2nd | Timeout Indication | There is at least 1 character in the FIFO but no character has been input to the FIFO or read from it for the last 4 character times. | Reading from the FIFO (Receiver Buffer Register) |
| 001 | 3rd | Transmitter Holding Register Empty | Transmitter Holding Register Empty | Writing to the Transmitter Holding Register or reading IIR |
| 000 | 4th | Modem Status | CTS, DSR, RI or DCD | Reading the Modem status register |

**FCR (UART1 FIFO CONTROL REGISTER, 0x2512)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:6 | URXFTRIG | Adjust the trigger level of Receiver FIFO. Interrupt occurs when FIFO receives the data byte based on this field's value below. For example, when URXFTRIG field is set to '3', interrupt does not occur until FIFO receives 14 bytes. When FIFO receives 14 byte, interrupt occurs.<br>0: 1byte<br>1: 4 byte<br>2: 8 byte<br>3: 14 byte | WO | 3 |
| 5:3 | | Reserved | RO | 0 |
| 2 | UTXFRST | When this field is set to '1', Transmitter FIFO is cleared and the circuits related to it are reset. | WO | 0 |
| 1 | URXFRST | When this field is set to '1', Receiver | WO | 0 |

| | | | | |
|---|---|---|---|---|
| | | FIFO is cleared and the circuits related to it are reset. | | |
| 0 | | Reserved | RO | 0 |

**LCR (UART1 LINE CONTROL REGISTER, 0x2513)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | DLAB | Divisor Latch Access Enable.<br>When this field is set to '1', Divisor register (DLM, DLL) can be accessed. When this field is set to '0', general register can be accessed. | R/W | 0 |
| 6 | SB | Set Break.<br>When this field is set to '1', serial output is forced to be '0'(break state). | R/W | 0 |
| 5 | SP | Stick Parity.<br>When PEN and EPS are '1' while this field set to '1', a parity of '0' is transmitted. In reception mode, it checks whether parity value is '0' or not.<br>When PEN is '1' and EPS is '0' while this field is to '1', parity of '1', is transmitted. In reception mode, it checks whether parity value is '1' or not. | R/W | 0 |
| 4 | EPS | Even Parity Enable.<br>When this field is set to '1', parity value is even.<br>When set to '0', parity value is odd. | R/W | 0 |
| 3 | PEN | Parity Enable.<br>When this field is set to '1', parity is calculated for the byte to be transmitted and transferred with it. In reception mode, checks parity. When this field is '0', parity is not generated. | R/W | 0 |
| 2 | STB | Number of Stop Bits.<br>When this field is set to '1', 2 stop bit is used.<br>When transmitting a word (character) of 5 bit length, 1.5 stop bit is used.<br>When this field is '0', 1 stop bit is used. | R/W | 0 |
| 1:0 | WLS | Word Length Select.<br>0: 5bit Word<br>1: 6bit Word<br>2: 7bit Word<br>3: 8bit Word | R/W | 3 |

**LSR (UART1 LINE STATUS REGISTER, 0x2515)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | ERCVR | Error in Receiver Indicator.<br>1: At least one parity error, framing error or break indications have been received. | RO | 0 |

| | | | | |
|---|---|---|---|---|
| | | The bit is cleared upon reading from the register.<br>0: Otherwise. | | |
| 6 | TEMT | Transmitter Empty indicator.<br>1: Both the transmitter FIFO and transmitter shift register are empty. The bit is cleared when data is being been written to the transmitter FIFO.<br>'0': Otherwise. | RO | 1 |
| 5 | THRE | Transmit FIFO is empty.<br>1: The transmitter FIFO is empty. Generates Transmitter Holding Register Empty interrupt. The bit is cleared when data is being been written to the transmitter FIFO.<br>0: Otherwise. | RO | 1 |
| 4 | BI | Break Interrupt (BI) indicator.<br>1: A break condition has been reached in the current character. The break occurs when the line is held in logic 0 for a time of one character (start bit + data + parity + stop bit). In that case, one zero character enters the FIFO and the UART waits for a valid start bit to receive next character. The bit is cleared upon reading from the register. Generates receiver Line Status interrupt.<br>0: No break condition in the current character. | RO | 0 |
| 3 | FE | Framing Error (FE) indicator.<br>1: The received character at the top of the FIFO did not have a valid stop bit. Of course, generally, it might be that all the following data is corrupt. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt.<br>0: No framing error in the current | RO | 0 |

| | | | | |
|---|---|---|---|---|
| | | character. | | |
| 2 | PE | Parity Error (PE) indicator.<br>1: The character that is currently at the top of the FIFO has been received with parity error. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt.<br>0: No parity error in the current character. | RO | 0 |
| 1 | OE | Overrun Error (OE) indicator.<br>1: If the FIFO is full and another character has been received in the receiver shift register. If another character is starting to arrive, it will overwrite the data in the shift register but the FIFO will remain intact. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt.<br>0: No overrun state | RO | 0 |
| 0 | DR | Data Ready (DR) indicator.<br>0: No characters in the FIFO.<br>1: At least one character has been received and is in the FIFO. | RO | 0 |

**XCR (UART1 CLOCK DIVISOR REGISTER, 0x2517)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | XCR | This register can be accessed only when DLAB bit in LCR register is set to '1'. This register consists of 8 bit register. XCR register with DLM and DLL registers used in UART baudrate generation. | R/W | 0x10 |

**ECR (UART1 EXTRA FEATURE CONTROL REGISTER, 0x2515)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:3 | | Reserved. | RO | 0 |
| 2:0 | ECR | Extra feature control register.<br>0: Default register access.<br>2: RX FIFO Interrupt level (RIL) register access enable.<br>5: TX FIFO level count (TLC) register and RX FIFO level count (RLC) register access enable. | WO | 0 |

**TLC (UART1 TX FIFO LEVEL COUNT REGISTER, 0x2513)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | TXLVLCNT | This register can be accessed when ECR register is set to '5'. This register indicates filled data size in the TX FIFO | RO | 0x00 |

**RIL (UART1 RX FIFO INTERRUPT LEVEL REGISTER, 0x2514)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | RXINTLVL | This register can be accessed when ECR register is set to '2'. when RIL register is set to zero value, the URXFTRIG field of FCR is valid. If RIL register is set to non-zero value, the receiver FIFO interrupt occurs when received bytes is greater than or equal to RIL register value. | R/W | 0x00 |

**RLC (UART1 RX FIFO LEVEL COUNT REGISTER, 0x2514)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | RXLVLCNT | This register can be accessed when ECR register is set to '5'. This register indicates filled data size in the RX FIFO. | RO | 0x00 |

**VSPMUX (I2S SOURCE PATH MUX CONTROL REGISTER, 0x277F)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:3 | | Reserved. | RO | 0 |
| 2:0 | VSPMUX | when VSPMUX register set to '2'. Otherwise, UART1 FIFO size is 16 entry. The detailed information is in the I2S Part. | R/W | 0 |

## 8.8. SPI MASTER/SLAVE

During an SPI transmission, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The operation is different in either Master mode or Slave mode

In the Master mode, the data transmission is done by writing to the SPDR (SPI Data Register, 0x2542).
After transmission, data reception is initiated by a byte transmitted to the Slave device from the Master SPI clock. When the SPI interrupt occurs, the value of the SPDR register becomes the received data from the SPI slave device. Even though the SPDR TX and RX have the same address, no data collision occurs because the processes of writing and reading data happen sequentially.

In the Slave mode, the data must be ready in the SPDR when the Master calls for it. Data transmission is accomplished by writing to the SPDR before the SPI clock is generated by the Master. When the Master generates the SPI clock, the data in the SPDR of the Slave is transferred to the Master. If the SPDR in the Slave is empty, no data exchange occurs. Data reception is done by reading the SPDR when the next SPI interrupt occurs.

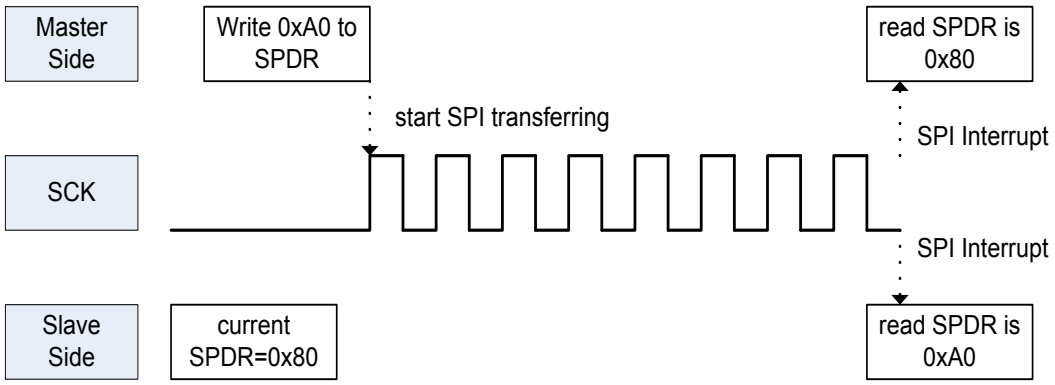



**Figure 15. SPI Data Transfer**

**SPCR (SPI CONTROL REGISTER, 0x2540)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | SPIE | SPI Interrupt Enable.<br>When this field is set to '1', SPI interrupt is enabled. | R/W | 0 |
| 6 | SPE | SPI Enable.<br>When this field is set to '1', SPI is enabled. | R/W | 0 |
| 5 | | Reserved | RO | 0 |
| 4 | MSTR | Master Mode Select.<br>When this field is set to '1', a Master mode is selected. | R/W | 1 |
| 3 | CPOL | Clock Polarity.<br>If there is no data transmission while this field is set to '0', SCK pin retains '0'.<br>If there is no data transmission while this field is set to '1', SCK pin retains '1'.<br>This field is used to set the clock and data between a Master and Slave with CPHA field.<br>Refer to the below for a more detailed explanation. | R/W | 0 |
| 2 | CPHA | Clock Phase.<br>This field is used to set the clock and data between a Master and Slave with CPOL field. | R/W | 0 |
| 1:0 | SPR | SPI Clock Rate Select.<br>With ESPR field in SPER register(0x2543), selects SPI clock(SCK) rate when the device is configured as a Master.<br>Refer to the ESPR field below. | R/W | 0 |

There are four methods of data transfer based on the settings of CPOL and CPHA. Polarity of SPI serial clock(SCK) is determined by CPOL value and it determines whether SCK activates high or low.

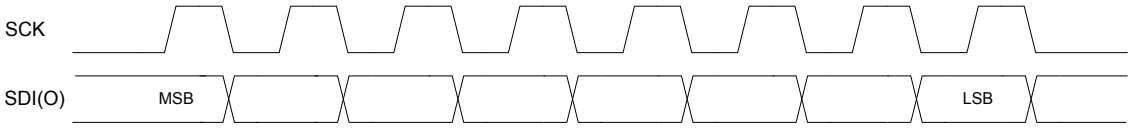
If CPOL value is '0', SCK pin retains '0' during no data transmission. If CPOL value is '1',

SCK pin retains '1' during no data transmission. CPHA field determines the format of data to be transmitted.

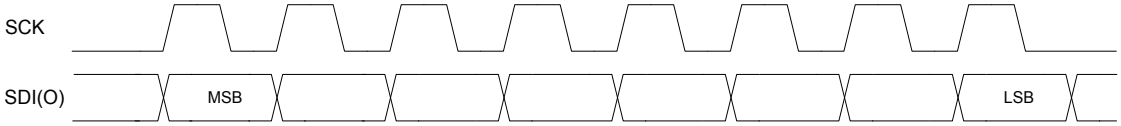
The table below describes the clock polarity and the data transition timing.

| CPOL | CPHA | SCK when idle | Data Transition Timing |
|---|---|---|---|
| 0 | 0 | Low | Falling Edge of SCK |
| 0 | 1 | Low | Rising Edge of SCK |
| 1 | 0 | High | Rising Edge of SCK |
| 1 | 1 | High | Falling Edge of SCK |

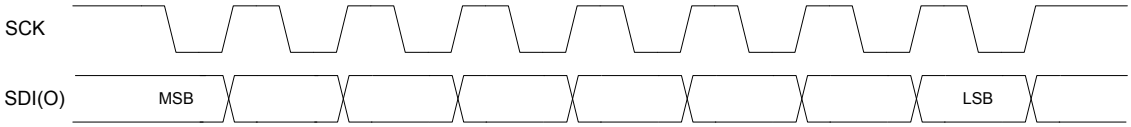
The following describes this block when slave mode is selected. When the values of CPOL and CPHA are the same, (a) and (b) below, output data is changed at the falling edge of SCK. Input data is captured at the rising edge of SCK. When the CPOL and CPHA values are different, (b) and (c) below, output data is changed at the rising edge of received SCK. Input data is captured at the falling edge of SCK.



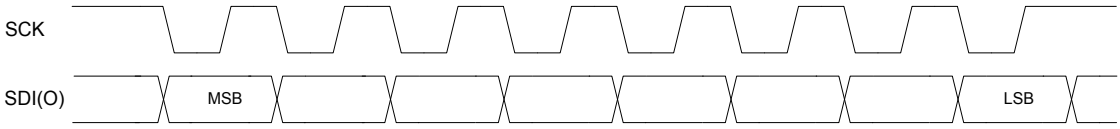
(a) CPOL=0, CPHA=0



(b) CPOL=0, CPHA=1



(c) CPOL=1, CPHA=0



(d) CPOL=1, CPHA=1

**SPSR (SPI STATUS REGISTER, 0x2541)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | SPIF | SPI Interrupt Flag.<br>When SPI interrupt occurs, this field is set to '1'. Set whenever data transmission is finished and it can be cleared by software. | R/W | 0 |
| 6 | WCOL | Write Collision.<br>This field is set to '1' when writing data to the SPDR register while SPITX FIFO is full.<br>It can be cleared by software. | R/W | 0 |
| 5:4 | | Reserved | RO | 0 |
| 3 | WFFUL | Write FIFO Full. | RO | 0 |

| | | | | |
|---|---|---|---|---|
| | | This field is set to '1' when Write FIFO is full.<br>This field is read only. | | |
| 2 | WFEMPTY | Write FIFO Empty.<br>This field is set to '1' when Write FIFO is cleared. This field is read only. | RO | 1 |
| 1 | RFFUL | Read FIFO Full.<br>This field is set to '1' when Read FIFO is full.<br>This field is read only. | RO | 0 |
| 0 | RFEMPTY | Read FIFO Empty.<br>This field is set to '1' when Read FIFO is cleared. This field is read only. | RO | 1 |

**SPDR (SPI DATA REGISTER, 0x2542)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | SPDR | This register is read/write buffer. | R/W | - |

**SPER (SPI E REGISTER, 0x2543)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:6 | ICNT | Interrupt Count.<br>This field indicates the number of byte to transmit. SPIF bit is set to '1' whenever each byte is transmitted. | R/W | 0 |
| 5:2 | | Reserved | RO | 0 |
| 1:0 | ESPR | Extended SPI Clock Rate Select.<br>With SPR field in SPCR Register (0x2540), this field selects SPI clock(SCK) rate when a device is configured as a Master.<br><br>{ESPR, SPR} / (System Clock Divider)<br>0000 Reserved<br>0001 Reserved<br>0010 8<br>0011 32<br>0100 64<br>0101 16<br>0110 128<br>0111 256<br>1000 512<br>1001 1024<br>1010 2048<br>1011 4096<br>* ESPR field : high bit<br>SPR field: low bit | R/W | 2 |

The value of ESPR and SPR is used to divide system clock to generate SPI clock (SCK). For example, if the value of ESPR and SPR is '0010' and system clock is 8MHz, SPI clock (SCK) is 1MHz.

**VSPMUX (I2S SOURCE PATH MUX CONTROL REGISTER, 0x277F)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:3 | | Reserved. | RO | 0 |
| 2:0 | VSPMUX | When VSPMUX register set to '3'. SPI FIFO size is changed 256 entries. Otherwise, SPI FIFO size is 16 entries. The detailed information is in the I2S Part. | R/W | 0 |

## 8.9. I2C MASTER/SLAVE

I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. It is most suitable for applications requiring occasional communication over a short distance between many devices.
Devices controlling the buses are called as Master. Master is responsible for generation of bus control and synchronizing signals. Slaves just follow the Master. Any I2C device can be either receiver or transmitter. The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

I2C core serves both as I2C compatible master and slave. This core supports the following functionalities:

- Both Master and slave operation
- Both Interrupt and non interrupt data-transfers
- Start/Stop generation
- Software programmable acknowledge bit
- Software programmable time out feature
- programmable address register
- Programmable SCL frequency
- Soft reset of I2C Master/Salve
- Programmable maximum SCL low period

**I2C_PRER (I2C PRESCALER REGISTER, 0x2794)**
I2C_PRER is used to pre-scale the SCL clock line.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | PRER | Prescaler for Master SCL generation | R/W | 0x10 |

I2C Maximum Transmission Rate
$f_{SCL}$ = $f_{sys}$ /(I2C_PRER*2+4) ($f_{sys}$ : I2C block system clock, default 8MHz)

The 4 extra cycles are for clock synchronization and the LOW to HIGH transition of SCL can be delayed if the device with the longest LOW period of SCL line is connected to the I2C bus.

**I2C_CTR (I2C CONTROL REGISTER, 0x2792)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | CENB | I2C Core Enable(0:enabled, 1:disabled) | R/W | 1 |
| 6 | INTE | Interrupt Enable (1:enabled, 0:disabled) | R/W | 0 |
| 5 | MS | I2C Mode Selection(1: Master, 0:Slave) | R/W | 0 |
| 4 | START/STOP | Select the START/STOP condition | R/W | 0 |

| | | | | |
|---|---|---|---|---|
| | | generation under the master mode.<br>Changing this bit from 0 to 1, START condition is generated.<br>Changing this bit from 1 to 0, STOP condition is generated. | | |
| 3 | REP_ST | When set to 1, a repeated START condition is generated.<br>If master wish to make another transfer immediately after the current, it can start a new transfer directly by transmitting a repeated START condition instead of a STOP followed by a START.<br>Please refer to [Figure 16] below. | R/W | 0 |
| 2 | NACK_GEN | NACK Generate | R/W | 0 |
| 1 | RXFIFO_RST | Receive FIFO Reset. Auto Clear | R/W | 0 |
| 0 | TXFIFO_RST | Transmit FIFO Reset. Auto Clear | R/W | 0 |

I2C single byte write, then repeated start and single byte read.

The identifiers used are:

- ADDR- Address
- DATA – Data
- S – Start bit
- Sr – Repeated start bit
- P – Stop bit
- W/R- Read(1)/ Write(0)
- A – ACK
- N – NACK


**Figure 16. I2C single byte write, then repeated start and single byte read**

**I2C_DAT (I2C TRASMIT/RECEIVE DATA REGISTER, 0x2790)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | I2C_DAT | read only for received data. write only for send data | R/W | - |

**I2C_ADDR (I2C SLAVE ADDRESS REGISTER, 0x2791)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | I2C_ADDR | Slave Address | R/W | 0xFF |

**I2C_STR (I2C INTERRUPT FLAG/STATUS REGISTER, 0x2793)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | ADDRESSED | Addressed flag<br>This bit will be set when address of the I2C matches the I2C_ADDR register in the slave mode or when a slave address is sent under the master mode.<br>At read, this bit is cleared. | RO | 0 |

| | | | | |
|---|---|---|---|---|
| 6 | MNACKED | Mastered Nacked flag<br>This bit indicates that I2C core detects the non-acknowledgement signal during the acknowledge clock pulse in the master mode.<br>At read, this bit is cleared. | RO | 0 |
| 5 | SNACKED | Slave Nacked Flag<br>This bit indicates that I2C core detects the non-acknowledgement signal during the acknowledge clock pulse in the slave mode.<br>At read, this bit is cleared. | RO | 0 |
| 4 | FINT | FIFO Interrupt flag<br>For the kinds of this flag, please refer to the I2C_FINTVAL (0x279E) register. | RO | 0 |
| 3 | BBUSY | Bus Busy flag<br>This indicates that I2C transfer is in progress and bus in not free. This bit will be set on detection of START condition and will be cleared on STOP condition.<br>At read, this bit is cleared. | RO | 0 |
| 2 | BTRANS | Byte Transferred flag<br>This bit indicates that one byte of data is being transferred. This bit will be 1 only after all 8bits is sent.<br>( 1: Byte transfer completed,<br>0: Byte transfer in progress )<br>At read, this bit is cleared. | RO | 0 |
| 1 | Reserved | - | | |
| 0 | TO | Time Out | RO | 0 |

**I2C_HOLD (I2C SCL/SDA HOLD CYCLE REGISTER, 0x2795)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:4 | CHOLD | SCL Hold Cycles | R/W | 0 |
| 3:0 | DHOLD | SDA Hold Cycles | R/W | 0 |

**I2C_TO (I2C TIME-OUT REGISTER, 0x2796)**

This register is for detecting the SCL clock low timeout condition.

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | TO | Time-Out Value | R/W | 0xFF |

If the current state of SCL stays LOW for a time period greater than time-out value set by I2C_TO register when transfer on the bus is active, the internal time-out reset is generated and the internal state of the I2C is reset, terminating any ongoing transfers. When this register value is 0xFF, the time-out function of SCL line is disabled.

**I2C_RXLVL (I2C RX FIFO INTERRUPT LEVEL REGISTER, 0x2797)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | RXLVL | RX FIFO Level Interrupt High Threshold | R/W | 0 |

**I2C_RXCNT (I2C RX FIFO CURRENT LEVEL REGISTER, 0x2798)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | RXCNT | RX FIFO Current Level | R/W | 0 |

**I2C_RXSTS (I2C RX FIFO STATUS REGISTER, 0x2799)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:6 | Reserved | | RO | 0 |
| 5 | OVF | RX FIFO Overflow | RO | 0 |
| 4 | FULL | RX FIFO Full | RO | 0 |
| 3 | LVL | RX FIFO Level Hit (RXCNT >= RXLVL) | RO | 0 |
| 2 | EMPT | RX FIFO Empty | RO | 1 |
| 1 | UDF | RX FIFO Underflow | RO | 0 |
| 0 | EMPT | RX FIFO Empty | RO | 1 |

**I2C_TXLVL (I2C TX FIFO INTERRUPT LEVEL REGISTER, 0x279A)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | TXLVL | TX FIFO Level Interrupt Low Threshold | R/W | 0 |

**I2C_TXCNT (I2C TX FIFO CURRENT LEVEL REGISTER, 0x279B)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | TXCNT | TX FIFO Current Level | R/W | 0 |

**I2C_TXSTS (I2C TX FIFO STATUS REGISTER, 0x279C)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:6 | Reserved | | RO | 0 |
| 5 | OVF | TX FIFO Overflow | RO | 0 |
| 4 | FULL | TX FIFO Full | RO | 0 |
| 3 | LVL | TX FIFO Level Hit (TXCNT <= TXLVL) | RO | 0 |
| 2 | EMPT | TX FIFO Empty | RO | 1 |
| 1 | UDF | TX FIFO Underflow | RO | 0 |
| 0 | EMPT | TX FIFO Empty | RO | 1 |

**I2C_FINTMSK (I2C FIFO INTERRUPT MASK REGISTER, 0x279D)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:4 | Reserved | - | RO | 0 |
| 3 | TXLVL | TX FIFO Level Interrupt Mask. When zero, The Interrupt is masked | R/W | 0 |
| 2 | TXEMPT | TX FIFO Empty Interrupt Mask. When zero, The Interrupt is masked | R/W | 0 |
| 1 | RXLVL | RX FIFO Level Interrupt Mask. When zero, The Interrupt is masked | R/W | 0 |
| 0 | RXRDA | RX FIFO Data Available Interrupt Mask. When zero, The Interrupt is masked | R/W | 0 |

**I2C_FINTVAL (I2C FIFO INTERRUPT FLAG REGISTER, 0x279E)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:4 | Reserved | - | RO | 0 |
| 3 | TXLVL | TX FIFO Level Interrupt Flag.<br>At read, this bit is cleared. | RO | 0 |
| 2 | TXEMPT | TX FIFO Empty Interrupt Flag.<br>At read, this bit is cleared. | RO | 0 |
| 1 | RXLVL | RX FIFO Level Interrupt Flag.<br>At read, this bit is cleared. | RO | 0 |
| 0 | RXRDA | RX FIFO Data Available Interrupt Flag.<br>At read, this bit is cleared. | RO | 0 |

**I2C_IMSK (I2C INTERRUPT MASK REGISTER, 0x279F)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | ADDRESSED | Addressed Interrupt Mask. When zero, The Interrupt is masked | R/W | 0 |
| 6 | MNacked | Master Nacked Interrupt Mask. When zero, The Interrupt is masked | R/W | 0 |
| 5 | SNacked | Slave Nacked Interrupt Mask. When zero, The Interrupt is masked | R/W | 0 |
| 4 | FINT | FIFO Level Interrupt Mask. When zero, The Interrupt is masked | R/W | 0 |
| 3 | BBUSY | Bus Busy Interrupt Mask. When zero, The Interrupt is masked | R/W | 0 |
| 2 | BTRANS | Byte Transfer Completed Interrupt Mask. When zero, The Interrupt is masked | R/W | 0 |
| 1 | Reserved | | RO | 0 |
| 0 | TO | Time Out Interrupt Mask. When zero, The Interrupt is masked | R/W | 0 |

## 8.10. IR(Infra-Red) Modulator

Embedded IR Modulator can support NEC PPM (Pulse Position Modulation) format transfer. The carrier duration and duty rate can be set by PPM_TCCNT, PPM_HCCNT. The data bit generation and the duty rate are set by PPM_T0CNT, PPM_H0CNT for bit pattern 0, and by PPM_T1CNT, PPM_H1CNT for bit pattern 1. The bit generation clock is generated by CDIV divisor.

$$Carrier\_Freq = \frac{fsystem}{TCCNT}$$

$$Carrier\_Duty = \frac{HCCNT}{TCCNT}$$

$$Bit0\_Duration = \frac{T0CNT * CDIV}{fsystem}$$

$$Bit0\_Duty = \frac{H0CNT}{T0CNT}$$

$$Bit1\_Duration = \frac{T1CNT * CDIV}{fsystem}$$

$$Bit1\_Duty = \frac{H1CNT}{T1CNT}$$

**LCODE (PPM LEADER CODE REGISTER, 0x27A0)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | LCODE | This register is read/write buffer. | R/W | 0x0F |

**PPM_SCODE (PPM STOP CODE REGISTER, 0x27A1)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | SCODE | This register is read/write buffer. | R/W | 0x00 |

**PPM_CCODE (PPM CUSTOM CODE REGISTER, 0x27A2)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | CCODE | This register is read/write buffer. | R/W | 0x00 |

**PPM_CCODB (PPM CUSTOM CODE BAR REGISTER, 0x27A3)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | CCODB | This register is read/write buffer. | R/W | 0xFF |

**PPM_DCODE (PPM DATA CODE REGISTER, 0x27A4)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | CCODE | This register is read/write buffer. | R/W | 0x00 |

### PPM_DCODB (PPM DATA CODE BAR REGISTER, 0x27A5)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | CCODB | This register is read/write buffer. | R/W | 0xFF |

### PPM_CTL (PPM CONTROL REGISTER, 0x27A6)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | EN | This register is read/write buffer. | R/W | 0 |
| 6 | DONE | TX Done. | RO | 0 |
| 5 | OE | Output Pin Enable | R/W | 0 |
| 4 | CONT | CONT generation | R/W | 0 |
| 3 | CPCC | Copy Custom Code Bar from PPM_CCODE register value | R/W | 1 |
| 2 | IVCC | Invert PPM_CCODE when CPCC=1 | R/W | 1 |
| 1 | CPDC | Copy Custom Code Bar from PPM_DCODE register value | R/W | 1 |
| 0 | IVDC | Invert PPM_DCODE when CPDC=1 | R/W | 1 |

### PPM_POSST (PPM DATA START POSITION REGISTER, 0x27A7)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | POSST | TX Start Bit Position | R/W | 0x08 |

### PPM_POSSP (PPM DATA STOP POSITION REGISTER, 0x27A8)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | POSSP | TX Stop Bit Position | R/W | 0x29 |

### PPM_TCCNT0 (PPM CARRIER DURATION COUNTER REGISTER, 0x27A9)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | TCCNT | PPM Carrier Duration Generation Counter. LSB Part | R/W | 0x4A |

### PPM_TCCNT1 (PPM CARRIER DURATION COUNTER REGISTER, 0x27AA)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 15:8 | TCCNT | PPM Carrier Duration Generation Counter. LSB Part | R/W | 0x03 |

### PPM_HCCNT0 (PPM CARRIER HIGH COUNTER REGISTER, 0x27AB)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | HCCNT | PPM Carrier High Duration Counter. LSB Part | R/W | 0x18 |

### PPM_HCCNT1 (PPM CARRIER HIGH COUNTER REGISTER, 0x27AC)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 15:8 | HCCNT | PPM Carrier High Duration Counter. MSB Part. | R/W | 0x01 |

### PPM_T0CNT (PPM BIT0 DURATION COUNTER REGISTER, 0x27AD)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | T0CNT | PPM Data Bit Pattern 0 Duration Counter | R/W | 0x20 |

**PPM_T1CNT (PPM BIT1 DURATION COUNTER REGISTER, 0x27AE)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | T1CNT | PPM Data Bit Pattern 1 Duration Counter | R/W | 0x40 |

**PPM_H0CNT (PPM DATA CODE BAR REGISTER, 0x27AF)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | H0CNT | PPM Data Bit Pattern 0 High Duration Counter | R/W | x010 |

**PPM_H1CNT (PPM DATA CODE BAR REGISTER, 0x27B0)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | H1CNT | PPM Data Bit Pattern 1 High Duration | R/W | 0x10 |

**PPM_CDIV0 (PPM DATA BAUDRATE DIVISOR REGISTER, 0x27B1)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | CDIV0 | PPM Data Baud-rate Generate Divisor. LSB Part | R/W | 0x65 |

**PPM_CDIV1 (PPM DATA BAUDRATE DIVISIOR REGISTER, 0x27B2)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | CDIV1 | PPM Data Baud-rate Generate Divisor. MSB Part | R/W | 0x04 |

## 8.11. I2S

The I2S function includes the following:

- I2S Interface
- I2S FIFO
- DMA

The data generated through an external ADC is input to the I2S FIFO block in the MG2471 via an I2S interface. Data received via I2S stored in the I2S TXFIFO. The data is then transferred to the MAC TX FIFO through DMA operation and finally transmitted through the PHY layer.

By contrast, received data in the MAC RX FIFO is transferred to the I2S RXFIFO. It is finally transferred to an external DAC via I2S interface.

### 8.11.1. I2S

In I2S interface, data is transferred MSB first from the left channel, and then from the right channel. There are two ways to send data via I2S TX: writing data to the register by software, or by hardware. This is enabled by using POP field in STXMODE (0x252d). Similarly, there are two ways to receive data via I2S RX: the first is reading the register by software, and the other is by the PUSH field in SRXMODE (0x253d).
There are three methods in I2S interface as follows;

- I2S mode
- Left Justified mode
- Right Justified mode

In I2S mode, left channel data is transferred in order. When left channel data is transferred, LRCK value is ‘0’ and when right channel data is transferred, LRCK value is ‘1’. Transferred data and LRCK is changed at the falling edge. Refer to the (a) below.

In Left Justified mode, left channel data is transferred whenever LRCK=1 and right channel data is transferred, whenever LRCK=0. LRCK is changed at the falling edge of BLCK. Transferred data is changed at the rising edge of BCLK. Refer to the (b) below.

In Right Justified mode, left channel data allows last LSB to be output before LRCK value goes to ‘0’ and right channel data allows last LSB to be output before LRCK value goes to ‘1’. LRCK value is changed at the falling edge of BCLK. Output data is changed at the rising edge of BCLK. Refer to the (c) below.

The following shows the interface method for each mode and I2S TX block is selected as Master. The setting of register is as follows. MS field in STXAIC (0x2528) register is set to ‘1’. WL field is set to ‘0’(The data of left and right channel represents 16-bit). Other fields are set to ‘0’. In I2S mode, BCP field in STXAIC (0x2528) register is set to ‘0’. In other modes, BCP field in STXAIC (0x2528) register is set to ‘1’.

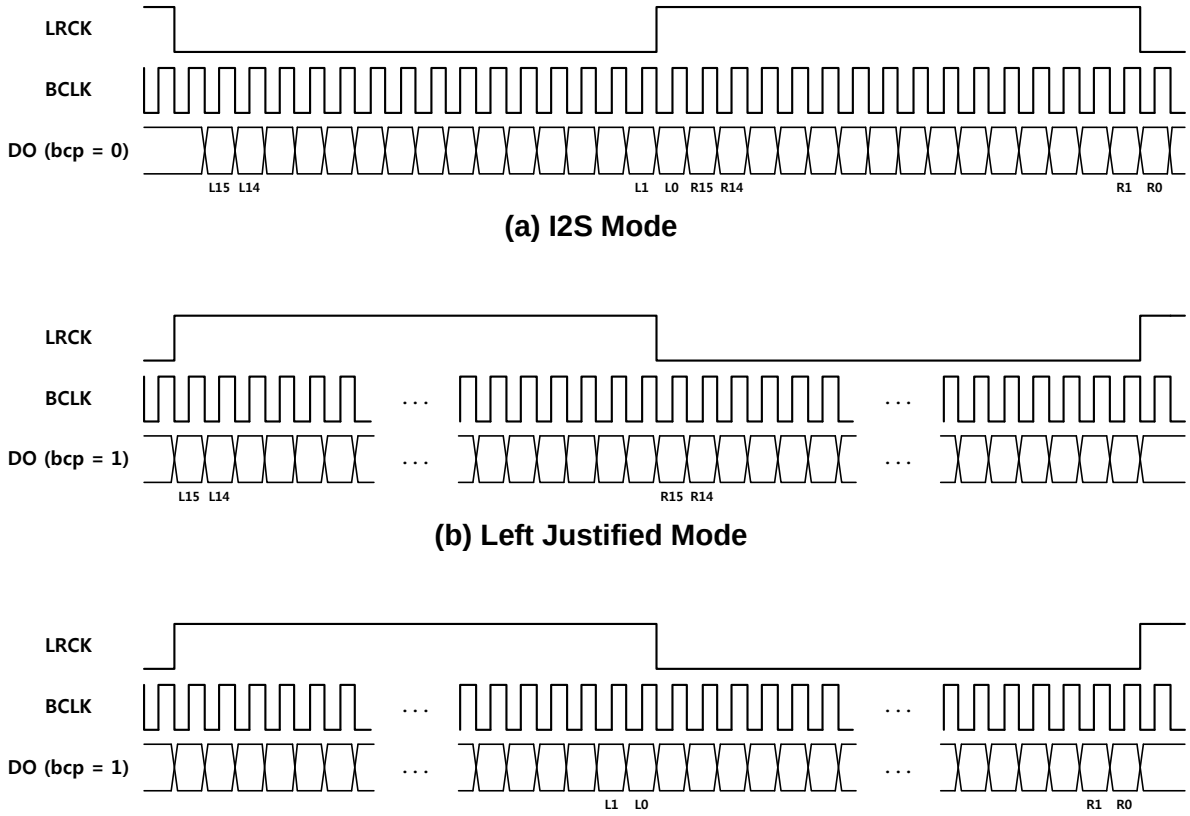



**Figure 17. Three Methods in I2S Interface**

**Note :** The number of BCLK should be greater than or equal to the configured data word-length.

**STXAIC (I2S TX INTERFACE CONTROL REGISTER, 0x2528)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | MS | When this field is set to '1', Master mode is configured. When this field is set to '0', Slave mode is configured.<br>Any device can act as the system master by providing the necessary clock signals. A slave will usually derive its internal clock signal from an external clock input. | R/W | 1 |
| 6:5 | FMT | Three modes of operation determined by the value of this field below.<br>0: I2S mode<br>1: Right Justified mode<br>2: Left Justified mode<br>3: Reserved | R/W | 2 |
| 4:3 | WL | Word Length.<br>This field indicates the number of bits per channel.<br>0: 16 bit<br>1: Reserved<br>2: 24 bit<br>3: 32 bit | R/W | 0 |
| 2 | LRSWAP | Left/Right Swap. | R/W | 0 |

| | | | | |
|---|---|---|---|---|
| | | When this field is set to '1', the order of the channel for transmitting data is changed.<br>In other words, the data in a right channel is transmitted first. | | |
| 1 | FRAMEP | When this field is set to '1', the polarity of LRCK is changed. For example, in Left Justified mode, the left channel data is outputted when LRCK=1 and the right channel data is outputted when LRCK=0. However, when this field is set to '1', the right channel data is outputted when LRCK=1 and the left channel data is outputted when LRCK=0. | R/W | 0 |
| 0 | BCP | When this field is set to '1', the polarity of BCLK(Bit Clock) is changed.<br>Clock edge, which allows the data change, is changed. | R/W | 0 |

**STXSDIV (I2S TX SYSTEM CLOCK DIVISOR REGISTER, 0x252A)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | STXSDIV | This register sets the value for dividing a system clock to generate MCLK.<br>The equation is as follows:<br>MCLK = System Clock/(2×STXSDIV)<br>When this field is '0', MCLK is not generated. | R/W | 0x00 |

**STXMDIV (I2S TX MCLK DIVISOR REGISTER, 0x252B)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | STXMDIV | This register sets the value for dividing MCLK to generate BCLK.<br>When STXSDIV register value is '1', BCLK = MCLK/STXMDIV. When STXSDIV register value is greater than 2, BCLK = MCLK/(2×STXMDIV).<br>When this register value is '0', BCLK is not generated. | R/W | 0x00 |

**STXBDIV (I2S TX BCLK DIVISOR REGISTER, 0x252C)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | STXBDIV | This register sets the value for dividing BCLK to generate LRCK.<br>LRCK = BCLK/(2×STXBDIV).<br>When this register value is '0', LRCK is not generated. | R/W | 0x00 |

**STXMODE (I2S TX MODE REGISTER, 0x252D)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | CSHR | This field is meaningful when I2STX block acts in a Slave mode.<br>When this field is set to '1', I2S TX block shares the clock of I2S RX block.<br>In other words, the MCLK of the I2S RX block is input to the MCLK of the I2S TX block and BCLK of I2S RX block is input to the BCLK of I2S TX block. As well, LRCK of I2S RX block | R/W | 0 |

| | | | | |
|---|---|---|---|---|
| | | is input to the LRCK of I2S TX block. | | |
| 6 | MPOL | This field determines the polarity of MCLK.<br>When this field is '0', MCLK signal retains '1'.<br>When this field is '1', MCLK signal retains '0'. | R/W | 1 |
| 5 | BPOL | This field indicates the relationship between BCLK and LRCK.<br>When this field is set to '0', LRCK value is changed at the falling edge of BCLK.<br>When this field is set to '1', LRCK value is changed at the rising edge of BCLK.<br>When FMT field in STXAIC(0x2528) register is '0', following configurations are restricted. (BCP field in STXAIC register)<br>BPOL = 0, BCP = 1<br>BPOL = 1, BCP = 0<br>When FMT field is ' 1', ' 2', following configurations are restricted.<br>BPOL = 0, BCP = 0<br>BPOL = 1, BCP = 1 | R/W | 1 |
| 4 | B16 | This field determines bit width to transfer data in I2S block to I2S block.<br>When this field is set to '1', data is transferred by 16-bit data format to I2S block.<br>When this field is set to '0', data is transferred by 8-bit data format to I2S block. | R/W | 1 |
| 3 | POP | When this field is set to '1', data is transferred to I2S block.<br>When this field is set to '0', data is not transferred to I2S block. | R/W | 1 |
| 2:1 | MODE | This field sets the mode of transferred data.<br>0: BLK Mode. Transfer a '0'.<br>1: MRT Mode.<br>Only the data in Right channel is transferred.( '0' is transferred in Left channel)<br>2: MLT Mode.<br>Only the data in Left channel is transferred.('0' is transferred in Right channel)<br>3: STR Mode.<br>All data in Left or Right channel are transferred. | R/W | 3 |
| 0 | CLKENA | Clock Enable.<br>When this field is set to '1', I2S TX is enabled. | R/W | 0 |

**SRXAIC (I2S RX INTERFACE CONTROL REGISTER, 0x2538)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | MS | When this field is set to '1', Master mode is configured. When this field is set to '0', Slave mode is configured.<br>Any device can act as the system master by providing the necessary clock signals. A slave will usually derive its internal clock signal from an external clock input. | R/W | 1 |
| 6:5 | FMT | Three modes determined by the value of this field below.<br>0: I2S mode<br>1: Right Justified mode<br>2: Left Justified mode | R/W | 2 |

| | | | | |
|---|---|---|---|---|
| | | 3: Reserved | | |
| 4:3 | WL | Word Length.<br>This field indicates the number of bit per each channel.<br>0: 16 bit<br>1: 20 bit<br>2: 24 bit<br>3: 32 bit | R/W | 0 |
| 2 | LRSWAP | Left/Right Swap.<br>When this field is set to '1', the order of the channel for transmitting data is changed.<br>In other words, the data in a right channel is transmitted first. | R/W | 0 |
| 1 | FRAMEP | When this field is set to '1', the polarity of LRCK is changed. For example, in Left Justified mode(FMT=2), data is stored in the left channel when LRCK=1 and data is stored in the right channel when LRCK=0. However, when this field is set to '1', data is stored in the right channel when LRCK=1 and the data is stored in the left channel when LRCK=0. | R/W | 0 |
| 0 | BCP | When this field is set to '1', the polarity of BCLK(Bit Clock) is changed.<br>Clock edge, which allows the data change, is changed. | R/W | 0 |

### SRXSDIV (I2S RX SYSTEM CLOCK DIVISOR REGISTER, 0x253A)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | SRXSDIV | This register sets the value for dividing a system clock to generate MCLK.<br>The equation is as follows:<br>MCLK = System Clock/(2× SRXSDIV)<br>When this field is '0', MCLK is not generated. | R/W | 0x00 |

### SRXMDIV (I2S RX MCLK DIVISOR REGISTER, 0x253B)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | SRXMDIV | This register sets the value for dividing MCLK to generate BCLK.<br>When SRXSDIV register value is '1', BCLK = MCLK/SRXMDIV. When SRXSDIV register value is greater than 2, BCLK = MCLK/(2×SRXMDIV).<br>When this register value is '0', BCLK is not generated. | R/W | 0x00 |

### SRXBDIV (I2S RX BCLK DIVISOR REGISTER, 0x253C)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | SRXBDIV | This register sets the value for dividing BCLK to generate LRCK. LRCK = BCLK/(2(SRXBDIV). When this register value is '0', LRCK is not generated. | R/W | 0x00 |

**SRXMODE (I2S RX MODE REGISTER, 0x253D)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | CSHR | This field is meaningful when I2SRX block acts in a Slave mode.<br>When this field is set to '1', I2S RX block shares the clock of I2S TX block.<br>In other words, MCLK of I2S TX block is input to the MCLK of I2S RX block and BCLK of I2S TX block is input to the BCLK of I2S RX block. As well, LRCK of I2S TX block is input to the LRCK of I2S RX block. | R/W | 0 |
| 6 | MPOL | This field determines the polarity of MCLK.<br>When this field is '0', MCLK signal retains '1'.<br>When this field is '1', MCLK signal retains '0'. | R/W | 0 |
| 5 | BPOL | This field indicates the relationship between BCLK and LRCK.<br>When this field is set to '0', LRCK value is changed at the falling edge of BCLK.<br>When this field is set to '1',LRCK value is changed at the rising edge of BCLK. | R/W | 0 |
| 4 | B16 | This field determines bit width to transfer data received from external ADC via I2S interface to I2S block.<br>When this field is set to '1', data is transferred by 16-bit data format to I2S block.<br>When this field is set to '0', data is transferred by 8-bit data format to I2S block. | R/W | 0 |
| 3 | PUSH | When this field is set to '1', data received from external ADC via I2S interface is transferred to I2S block.<br>When this field is set to '0', data received from external ADC via I2S interface is not transferred to I2S block. | R/W | 0 |
| 2:1 | MODE | This field sets the mode of transferred data.<br>0: BLK Mode. Transfer a '0'.<br>1: MRT Mode.<br>Only the data in Right channel is transferred.( '0' is transferred in Left channel)<br>2: MLT Mode.<br>Only the data in Left channel is transferred.( '0' is transferred in Right channel)<br>3: STR Mode.<br>All data in Left or Right channel are transferred. | R/W | 0 |
| 0 | CLKENA | Clock Enable.<br>When this field is set to '1', I2S RX is enabled. | R/W | 0 |

### 8.11.2. I2S FIFO

Data received via I2S interface is stored in I2S TXFIFO (0x2800~0x28FF). The size of I2S TXFIFO is 256 byte.

Data in MAC RXFIFO is processed by DMA operation, and stored in I2S RX FIFO (0x2900~0x29FF). Data in I2S RXFIFO is transmitted to an external component via I2S. The size of I2S RXFIFO is 256 byte.

### 8.11.2.1. I2S TX FIFO CONTROL

**VTFDAT (I2S TX FIFO DATA REGISTER, 0x2750)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | VTFDAT | When writing data to this register, data is stored in I2S TX FIFO in order.<br>When reading this register, data stored in I2S TX FIFO can be read. | R/W | 0x00 |

**VTFMUT (I2S TX FIFO MUTE DATA REGISTER, 0x2751)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | VTFMUT | When MUT field in VTFCTL register is set to '1', data in this register is transferred instead of data in I2S TX FIFO.<br>When INI field in VTFCTL register is set to '1', data in I2S TX FIFO is initialized by data in VTFMUT. | R/W | 0x00 |

**VTFCTL (I2S TX FIFO CONTROL REGISTER, 0x2752)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:4 | | Reserved | RO | 0 |
| 3 | VTDENA | I2S TX DMA Enable.<br>When this field is set to '1', I2S TX DMA is enabled. This field value is cleared automatically. | WO | 0 |
| 2 | MUT | When this field is set to '1', data in VTFMUT register is transferred instead of data in I2S TX FIFO. This field can be read. | R/W | 0 |
| 1 | CLR | When this field is set to '1', Write pointer and Read pointer of I2S TX FIFO are initialized. The status value of underflow and overflow is initialized. | WO | 0 |
| 0 | INI | When this field is set to '1', all data in I2S TXFIFO is replaced by the value in VTFMUT register. | WO | 0 |

**VTFRP (I2S TX FIFO READ POINTER REGISTER, 0x2753)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | VTFRP | This register indicates the address of I2S TXFIFO to be read next. Since the size of FIFO is 256 byte, LSB is used to test wrap-around. | R/W | 0x00 |

**VTFWP (I2S TX FIFO WRITE POINTER REGISTER, 0x2754)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | VTFWP | This register indicates the address of I2S TXFIFO to be written next. Since the size of FIFO is 256 byte, LSB is used to test wrap-around. | R/W | 0x00 |

**VTFSTS (I2S TX FIFO STATUS REGISTER, 0x275A)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:5 | | Reserved | RO | 0 |
| 4 | ZERO | When INI field in VTFCTL register is set to '1', data in I2S TX FIFO is initialized by data in VTFMUT register. During this initialization is processed, this field is set to '1'. After initialization is finished, this field is set to '0'. | RO | 0 |
| 3 | PSH | This field is set to '1' while pushing data into I2S TX FIFO. | RO | 0 |
| 2 | POP | This field is set to '1' while popping data on I2S TX FIFO. | RO | 0 |
| 1:0 | | Reserved | | 0 |

**VTDSIZE (I2S TX DMA SIZE REGISTER(I2S TX FIFO->MAC TX FIFO), 0x275B)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | VTDSIZE | Set the data size for DMA operation. | R/W | 0x00 |

### 8.11.2.2. I2S RX FIFO CONTROL

**VRFDAT (I2S RX FIFO DATA REGISTER, 0x2760)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | VRFDAT | When writing data to this register, data is stored in I2S RX FIFO in order.<br>When reading this register, data stored in I2S RX FIFO can be read. | R/W | 0x00 |

**VRFMUT (I2S RX FIFO MUTE DATA REGISTER, 0x2761)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | VRFMUT | When MUT field in VRFCTL register is set to '1', data in this register is transferred instead of data in I2S RX FIFO.<br>When INI field in VRFCTL register is set to '1',data in I2S RX FIFO is initialized by data in VTFMUT. | R/W | 0x00 |

**VRFCTL (I2S RX FIFO CONTROL REGISTER, 0x2762)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:4 | | Reserved | RO | 0 |
| 3 | VRDENA | I2S RX DMA Enable.<br>When this field is set to '1', I2S RX DMA is enabled. This field value is cleared automatically | WO | 0 |
| 2 | MUT | When this field is set to '1', data in the VRFMUT register is transferred instead of data in the I2S RX FIFO. This field can be read. | R/W | 0 |
| 1 | CLR | When this field is set to '1', Write pointer and Read pointer of I2S RX FIFO are initialized. The status value of underflow and overflow is initialized. | WO | 0 |
| 0 | INI | When this field is set to '1', all data in I2S RXFIFO is replaced by the value in | WO | 0 |

| | | | | |
|---|---|---|---|---|
| | | VRFMUT register. | | |

**VRFRP (I2S RX FIFO READ POINTER REGISTER, 0x2763)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | VRFRP | This register indicates the address of I2S RXFIFO to be read next.<br>Since the size of FIFO is 256 byte, the LSB is used to test wrap-around. | R/W | 0x00 |

**VRFWP (I2S RX FIFO WRITE POINTER REGISTER, 0x2764)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | VRFWP | This register indicates the address of I2S RXFIFO to be written next. Since the size of FIFO is 256 byte, the LSB is used to test wrap-around | R/W | 0x00 |

**VRFSTS (I2S RX FIFO STATUS REGISTER, 0x276A)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:5 | | Reserved | RO | 0 |
| 4 | ZERO | When INI field in VRFCTL register is set to '1', data in the I2S TX FIFO is initialized by the data in the VRFMUT register. During the processing of this initialization, this field is set to '1', and set to '0' when initialization is finished. | RO | 0 |
| 3 | PSH | This field is set to '1' while pushing data into the I2S RX FIFO. | RO | 0 |
| 2 | POP | This field is set to '1' while popping data on the I2S RX FIFO. | RO | 0 |
| 1:0 | | Reserved | RO | 0 |

**VRDSIZE (I2S RX DMA SIZE REGISTER (MAC RX FIFO->I2S RX FIFO), 0x276B)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | VRDSIZE | Sets the data size for DMA. | R/W | 0x00 |

### 8.11.2.3. I2S INTERFACE CONTROL

**VTFINTENA (I2S TX FIFO INTERRUPT ENABLE REGISTER, 0x2770)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | EMPTY | I2S TX FIFO Empty Interrupt Enable | R/W | 0 |
| 6 | FULL | I2S TX FIFO Full Interrupt Enable | R/W | 0 |
| 5:0 | | Should be set as '0'. | | 0 |

**VRFINTENA (I2S RX FIFO INTERRUPT ENABLE REGISTER, 0x2771)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | EMPTY | I2S RX FIFO Empty Interrupt Enable | R/W | 0 |
| 6 | FULL | I2S RX FIFO Full Interrupt Enable | R/W | 0 |
| 5:0 | | Should be set as '0'. | | 0 |

### VDMINTENA (I2S DMA CONTROLLER INTERRUPT ENABLE REGISTER, 0x2772)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:5 | | Should be set as '0'. | | 0 |
| 4 | VTDDONE | I2S TX DMA Done Interrupt Enable | R/W | 0 |
| 3:1 | | Should be set as '0'. | | 0 |
| 0 | VRDDONE | I2S RX DMA Done Interrupt Enable | R/W | 0 |

### VTFINTSRC (I2S TX FIFO INTERRUPT SOURCE REGISTER, 0x2773)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | EMPTY | I2S TX FIFO Empty Interrupt Source. When EMPTY field in VTFINTENA register is set to '1' and EMPTY field in VTFINTVAL register is set to '1', this field is set to '1'. Cleared by software. | R/W | 0 |
| 6 | FULL | I2S TX FIFO Full Interrupt Source | R/W | 0 |
| 5:0 | | Reserved | RO | 0 |

### VRFINTSRC (I2S RX FIFO INTERRUPT SOURCE REGISTER, 0x2774)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | EMPTY | I2S RX FIFO Empty Interrupt Source | R/W | 0 |
| 6 | FULL | I2S RX FIFO Full Interrupt Source | R/W | 0 |
| 5:0 | | Reserved | RO | 0 |

### VDMINTSRC (I2S DMA CONTROLLER INTERRUPT SOURCE REGISTER, 0x2775)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:5 | | Should be set as '0'. | | 0 |
| 4 | VTDDONE | I2S TX DMA Done Interrupt Source | R/W | 0 |
| 3:1 | | Should be set as '0'. | | 0 |
| 0 | VRDDONE | I2S RX DMA Done Interrupt Source | R/W | 0 |

### VCECFG (I2S CONFIG REGISTER, 0x2779)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:6 | VRFCFG | I2S Rx FIFO Configuration<br>0: Reserved<br>1: Selected the R/W path by 8051 CPU<br>2: Reserved<br>3: Used as the I2S Rx FIFO | R/W | 0 |
| 5:4 | | This field must be set to 3 (11b) | R/W | 0 |
| 3:2 | VTFCFG | I2S Tx FIFO Configuration.<br>0: Reserved<br>1: Selected the R/W path by 8051 CPU<br>2: Reserved<br>3: Used as the I2S Tx FIFO | R/W | 0 |
| 1:0 | | This field must be set to 3 (11b) | R/W | 0 |

**VSPMUX (I2S SOURCE PATH MUX CONTROL REGISTER, 0x277F)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:3 | | Reserved. | R/W | 0 |
| 2:0 | VSPMUX | 0: The 256 bytes I2S RX/TX FIFO mapped to I2S RX/TX FIFO.<br>1: I2S RX/TX FIFO mapped to UART0 RX/TX FIFO.<br>2: I2S RX/TX FIFO mapped to UART1 RX/TX FIFO.<br>3: I2S RX/TX FIFO mapped to SPI RX/TX FIFO.<br>7: I2S RX/TX FIFO memory mapped to data memory area (0x1A00-0x1BFF). The data memory area can be extended by the register value. | R/W | 0 |

## 8.12. Random Number Generator(RNG)

The random number generator (RNG) generates 32-bit random number with seed. Whenever ENA bit in RNGC register is set to '1', the generated number is stored in RNGD3 ~ RNGD0 register.

**RNGD3 (RNG DATA3 REGISTER, 0x2550)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | RNGD3 | This register stores MSB (RNG[31:24]) of 32-bit random number. | RO | 0xB7 |

**RNGD2 (RNG DATA2 REGISTER, 0x2551)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | RNGD2 | This register stores 2nd MSB (RNG[23:16]) of 32-bit random number. | RO | 0x91 |

**RNGD1 (RNG DATA1 REGISTER, 0x2552)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | RNGD1 | This register stores 3rd MSB (RNG[15:8]) of 32-bit random number. | RO | 0x69 |

**RNGD0 (RNG DATA0 REGISTER, 0x2553)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | RNGD0 | This register stores LSB (RNG[7:0]) of 32-bit random number. | RO | 0xC9 |

**SEED3 (RNG SEED3 REGISTER, 0x2554)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | SEED3 | This register stores MSB (SEED[31:24]) of required seed to generate random number. | WO | - |

**SEED2 (RNG SEED2 REGISTER, 0x2555)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | SEED2 | This register stores 2nd MSB (SEED[23:16]) of required seed to generate random number. | WO | 0x00 |

**SEED1 (RNG SEED1 REGISTER, 0x2556)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | SEED1 | This register stores 3rd MSB (SEED[15:8]) of required seed to generate random number. | WO | 0x00 |

**SEED0 (RNG SEED0 REGISTER, 0x2557)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | SEED0 | This register stores LSB (SEED[7:0]) of required seed to generate random number. | WO | 0x00 |

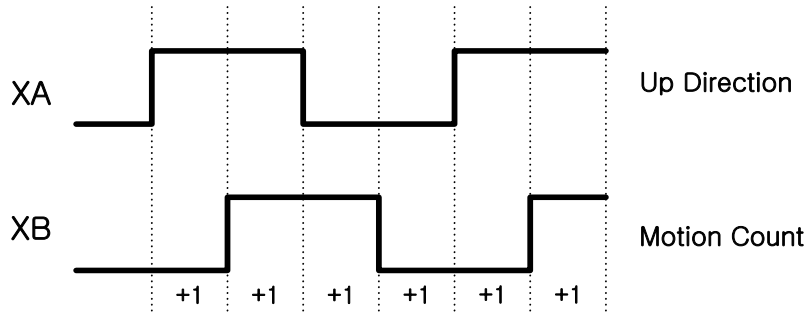
**RNGC (RNG DATA3 REGISTER, 0x2558)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:1 | | Reserved | RO | 0 |
| 0 | ENA | RNG Enable.<br>When this field is set to '1', RNG acts. This field value is changed to '0' automatically. | R/W | 0 |

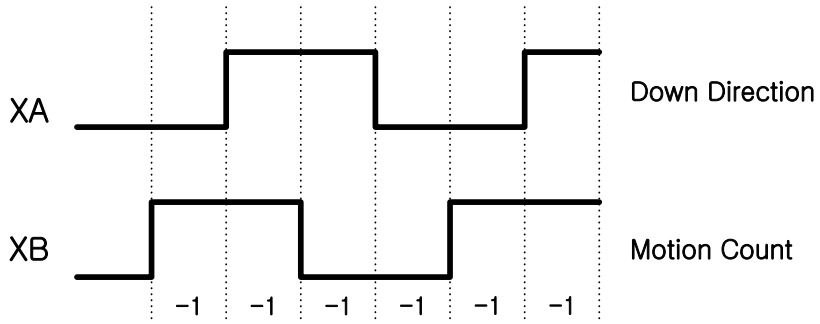
## 8.13. Quadrature Signal Decoder

The Quadrature Signal Decoder block notifies the MCU of the counter value based on the direction and movement of a pointing device, such as a mouse, after receiving Quadrature signal from the pointing device.
Quadrature signal is changed with 90° phase difference (1/4 period) between two signals as shown in [Figure 18]. In addition, counter value means 1/4 of one period. Since this block can receive three Quadrature signals, it can support not only the two-dimensional movement such as mouse but also the pointing device which is in three dimensions.

The (a) of [Figure 18] shows that the XA signal is changing before the XB signal. In this case, the pointing device is moving in the down direction. The (b) of [Figure 17] shows that XB signal is changing before XA signal. In this case, the pointing device is moving in the up direction. The rules for YA, YB, ZA and ZB are the same as described above for XA and XB.




**(a)**




**(b)**

**Figure 18. Quadrature signal timing between XA and XB**

### UDX (UpDown X Register, 0x2560)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:1 | | Reserved | RO | 0 |
| 0 | UPDN_X | This field notifies the MCU of movement in the X-axis direction.<br>1: Up<br>0: Down | RO | 0 |

### CNTX (Count X Register, 0x2561)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | CNTX | This field notifies the MCU of the count value for movement in the X-axis. | RO | 0x00 |

### UDY (UpDown Y Register, 0x2562)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:1 | | Reserved | RO | 0 |
| 0 | UPDN_Y | This field notifies the MCU of movement in the Y-axis.<br>1: Up<br>0: Down | RO | 0 |

### CNTY (Count Y Register, 0x2563)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | CNTY | This field notifies the MCU of the count value for movement in the Y-axis. | RO | 0x00 |

### UDZ (UpDown Z Register, 0x2564)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:1 | | Reserved | RO | 0 |
| 0 | UPDN_Z | This field notifies the MCU of movement in the Z-axis.<br>1: Up<br>0: Down | RO | 0 |

### CNTZ (Count Z Register, 0x2565)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | CNTZ | This field notifies the MCU of the count value for movement in the Z-axis. | RO | 0x00 |

**QCTL (Quad Control Register, 0x2566)**

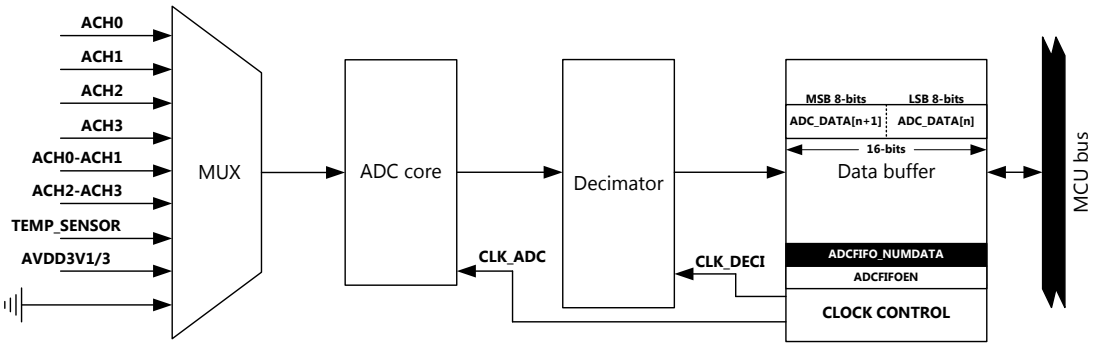
| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:3 | | Reserved | RO | 0 |
| 2 | ENA | Quad Enable.<br>When this field is set to '1', Quadrature Signal Decoder is enabled. | R/W | 0 |
| 1 | INI | Quad Initialize.<br>When this field is set to '1', internal register values of Quadrature Signal Decoder are initialized. | R/W | 1 |
| 0 | | Reserved | RO | 0 |

## 8.14. ADC

MG2471 supports the 4-channel ADC with 12bit resolution. The ADC includes an analog multiplexer with up to four individually configurable channels, sigma-delta modulator, decimator, and ADC FIFO. The converted values can be obtained by reading ADCVAL (0x22D7) twice.

The main features of the ADC are as follows;

- Selectable decimation rates and sampling clock
- Four individual input channels, single-ended or differential-ended
- Temperature sensor input
- Battery measurement capability




**PHY_CLK_EN1 (ADC CLOCK ENABLE REGISTER, 0x2781)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 3 | CLK_ADC_EN | ADC sampling clock on/off. The default value is 0(disabled). The clock rate selection among 1, 2, and 4MHz is done through register ADC_CLK_SEL(0x2786) | R/W | 0 |
| 2 | CLK_DECI_EN | The digital decimator clock on/off. The default value is 0(disabled). The clock rate of CLK_DECI is always 16MHz. | R/W | 0 |

**PHY_SW_RSTB (DECIMATOR RESET REGISTER, 0x2784)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 6 | RESETB_DECI | Active low reset for digital decimator. This | R/W | 1 |

| | | | | |
|---|---|---|---|---|
| | | register is not automatically cleared, so the register should be restored manually. | | |

### ADC_CLK_SEL (ADC SAMPLING RATE CONFIGURATION REGISTER, 0x2786)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 1:0 | ADC_CLK_SEL | The ADC sampling clock rate can be selected among 1, 2, and 4MHz (0x0=1MHz, 0x1=2MHz, 0x2=4MHz, 0x3=Not used) . | R/W | 0x2 |

### ADCNF1 (ADC CONFIGURATION1 REGISTER, 0x22D4)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | ADCEN | ADC core is activated when it is set to 1. | R/W | 0 |
| 6:4 | - | Reserved<br>Only '0x0' is allowed. | R/W | 0x0 |
| 3:0 | ADCHCNF | ADC channel selection.<br>0x0: ACH0<br>0x1: ACH1<br>0x2: ACH2<br>0x3: ACH3<br>0x4: ACH0 - ACH1<br>0x5: ACH2 - ACH3<br>0x6: Temperature sensor<br>0x7: Battery monitor(AVDD3V1)<br>0x8: GND<br>The configurations of 0x7 and 0x8 can be used the ADC calibration. | R/W | 0x0 |

### ADCNF2 (ADC CONFIGURATION2 REGISTER, 0x22D5)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:4 | ADCFIFOSIZE | The size of ADC FIFO. The number of available data in FIFO is ADCFIFOSIZE – 1. | R/W | 0xC |
| 3:2 | ADCOSRSEL | Oversampling ratio of ADC<br>0x0: Not used<br>0x1: 64x<br>0x2:128x<br>0x3: 256x | R/W | 0x3 |
| 1 | ADCFIFOEN | Data buffer mode selection.<br>0: normal delayed buffer, recent samples(ADCFIFOTHRINTR-1) samples are available in the ADC buffer(interrupt is not generated).<br>1: FIFO mode, when the buffer is full, the data is not stacked in the buffer(before the buffer is full, the data in the buffer should be read out). | R/W | 0 |

### ADCSTS (ADC STATUS MONITORING REGISTER, 0x22D6)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | - | Reserved | RO | 0 |
| 6:3 | ADCFIFO_NUMDATA | This field determines number of available data in buffer. Number of available data is ADCFIFO_NUMDATA – 1. The data ready check is possible by !(ADCSTS&0x70) | RO | 0x0 |
| 2:0 | - | Reserved | RO | 0x0 |

**ADCVAL (ADC CONVERSION RESULTS READ-OUT REGISTER, 0x22D7)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | ADC_DATA | The ADC values in 16bit can be obtained by reading this register twice. The LSB 8bit and MSB 8bit can be read sequentially.<br>Note: Effective resolution(12bit) is acquired by (MSB*256+LSB+8)/16 | RO | 0x00 |

## 8.15. Power Management

MG2471 has four operation modes to allow low power consumption. PM0 is the normal operating mode. The other 3 modes, PM1/PM2/PM3, are called power down modes.

Please note that MG2471 does not support the I/O retention mode at PM2 and PM3 because internal the digital regulator is off at entry of PM2 and PM3. At this time, each I/O pins are changed to input mode. MG2471 only supports the pull-up/down configuration retention of each IO pins under the power down modes. The pull-up/down configuration of each I/O pins can be set by GPIOPS0(0x22E7), GPIOPS1(0x22E8), GPIOPS3(0x22E9), GPIOPE0(0x22EA), GPIOPE1(0x22EB), and GPIOPE3(0x22EC) before entering the power down modes. The user of MG2471 should notice the above I/O pull-up/down configuration registers setting value to prevent the unnecessary leakage current consumption.

- **PM0**

PM0 is the normal operating mode where the RF transceiver, MCU, and peripherals are active. In PM0, all voltage regulators are on.

- **PM1**

PM1 is the power down mode where the 32MHz crystal oscillator and the 16MHz RC oscillator are powered down. The voltage regulator for digital core, the 32kHz oscillator, and the sleep timer are on. MG2471 wakes up from PM1 to PM0 by turning on the 16MHz RC oscillator and the 32MHz crystal oscillator when interrupts are occurred. MG2471 will run on the 16MHz RC oscillator and automatically switch clock source to the 32MHz crystal oscillator after the 32MHz crystal oscillator has settled.

- **PM2**

PM2 is the power down mode where the 32MHz crystal oscillator, the 16MHz RC oscillator, and the voltage regulator for digital core are powered down. In PM2, the 32kHz oscillator and the sleep timer are on. MG2471 wakes up from PM2 to PM0 by turning on the voltage regulator, the 16MHz RC oscillator, and the 32MHz crystal oscillator when interrupts are occurred. PM2 is used when it is relatively long until the expected time for wakeup event.

- **PM3**

PM3 is the power down mode where all clock oscillators, the voltage regulator, and sleep timer are powered down. MG2471 wakes up from PM3 to PM0 by turning on the voltage regulator, the 16MHz RC oscillator, and the 32MHz crystal oscillator when interrupts are occurred. PM3 is used to achieve ultra low power consumption.

- **Power Management Control**

Power down modes (PM1/PM2/PM3) can be set by PDMODE[1:0] in PDCON(0x22E0) register. After setting PDMODE, each power mode can be started by making PCON bit[1] to 1.
MG2471 will wake up from power down modes to PM0 by interrupts, which are the selected

I/O pins, the sleep timer, and the external reset.
All I/O pins can be set as wake up source by set GPIOMSK0(0x22F0), GPIOMSK1(0x22F1), and GPIOMSK3(0x22F2) and polarity of the I/O pins can be set by GPIOPOL0(0x22ED), GPIOPOL1(0x22EE), and GPIOPOL3(0x22EF).
Minimum operation time in PM0 must be over 30usec to re-enter into PM1/PM2/PM3.

## 8.16. Sleep Timer

Sleep timer is used to exit from the power down modes(PM1/PM2/PM3) The desired clock is generated from the 32kHz RC oscillator or inputs from an external 32.768kHz clock at P1[4] by setting SELRTCLK in PDCON(0x22E0). The sleep timer is activated as setting STEN bit in PDCON(0x22E0) to 1 and the interrupt interval can be programmed by setting RTINT1(0x22E3), RTINT2(0x22E4), RTINT3(0x22E5), and EXPRTVAL bits in PDMON(0x22E6). Sleep timer interval can be programmed by setting RTCPRDSEL in PDMON(0x22E6).
Sleep timer can be also used to RTC interrupt source in the normal operation mode(PM0).

When RTCPRDSEL in PDMON(0x22E6) is set to 1,
Sleep timer interval(sec) is calculated by 65536*EXPRTVAL[1:0] + RTVALSEC[15:0] + 3.904m*RTVALSUB[7:0]
When the RTCPRDSEL in PDMON(0x226) is set to 0,
Sleep timer interval(sec) is calculated by 512*EXPRTVAL[1:0] + 3.904m*RTVALSEC[15:0] + 30.5u*RTVALSUB[7:0] and minimum sleep timer interval must be over 71usec

## 8.17. 32kHz RC Oscillator

MG2471 has a low-power 32kHz RC oscillator for Sleep timer and watchdog timer. 32kHz RC oscillator is activated when RCOSCEN in PDCON(0x22E0) is set to 1. When the 32MHz crystal oscillator is selected and it is stable, i.e. OSCOK in PDMON(0x22E6) is 1, Frequency calibration of the 32kHz RC oscillator is continuously performed by setting RCCEN in RCOSCON(0x22E1). This calibration is performed in PM0 and retains the last calibration value in power down mode.

## 8.18. 32.768kHz Crystal Oscillator

The optional 32.768kHz crystal oscillator generates clock for sleep timer and watchdog timer. 32.768kHz crystal oscillator is activated when SELRTCLK in PDCON(0x22E0) is set to 1. When using 32.768kHz crystal oscillator, GPIO P1[3] and P1[4] must configure as high impedance input mode. Refer 8.2 for GPIO configuration.
P1[3] and P1[4] can accept an external digital clock input. If P1[3](P1[4]) is used for external digital clock input, P1[4](P1[3]) must be floating.
It is strongly recommended that 32.768kHz crystal unit should be closed to the chip to prevent increasing current consumption.

## 8.19. 16MHz RC Oscillator

MG2471 can run on the 16MHz RC oscillator until 32MHz crystal oscillator is stable for fast turn-on time. The 16MHz RC oscillator is activated when HSRCOSCEN in PDCON(0x22E0) is set to 1. When the 32MHz crystal oscillator is selected and it is stable, i.e. OSCOK in

PDMON(0x22E6) is 1, Frequency calibration of the 16MHz RC oscillator is continuously performed by setting HSRCCEN in RCOSCON(0x22E1). This calibration is performed in PM0 and retains the last calibration value in power down mode. The 16MHz RC oscillator consumes less power than the 32MHz crystal oscillator, but it cannot be used for RF transceiver operation.
The 16MHz RC oscillator is automatically turned off in the power down modes. When exiting from the power down mode, HSRCOSC_STS bit (CLKCON2, 0x8F) should be cleared in order to return to the normal mode and HSRCOSC_SEL bit (CLKCON1, 0x8E) should be set to 0 for switching the clock source to the 32MHz crystal oscillator.

## 8.20. 32MHz Crystal Oscillator

The crystal oscillator generates the reference clock for MG2471. An external 32MHz with two loading capacitors (C11 and C12) is used for the 32MHz crystal oscillator. The load capacitance seen by the 32MHz crystal is given by

$$C_L = \frac{1}{\frac{1}{C_{11}} + \frac{1}{C_{12}}} + C_{parasitic}$$

where $C_{parasitic}$ represents all parasitic capacitances such as PCB stray capacitance and the package pin capacitance.

## 8.21. Always-On Registers

All registers bits retain their previous values when entering PM2 or PM3.

**PDCON (POWER DOWN CONTROL REGISTER, 0x22E0)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | BODEN | It enables the Brown out detector(BOD), when DVDD1/DVDD2 falls under operation voltage.<br>1: Enables the Brown out detector.<br>0: Disables the Brown out detector. | R/W | 1 |
| 6 | AVREGEN | It controls voltage regulators in Analog part. It must be set to 0 before entering PM0/PM1/PM2<br>1: Enables voltage regulators in Analog part.<br>0: Disables voltage regulators in Analog part. | R/W | 1 |
| 5 | STEN | Register for controlling the sleep timer. When STEN is set to 1, the sleep timer operates by 32kHz RC oscillator or external 32.768kHz crystal oscillator.<br>1: Enables the sleep timer.<br>0: Disables the sleep timer. | R/W | 0 |
| 4 | HSRCOSCEN | It decides oscillation of the 16MHz RC oscillator. The 16MHz RC oscillator is used for fast turn on from PM1/2/3 or initial power up sequence.<br>1: Enables the 16MHz RC oscillator.<br>0: Disables the 16MHz RC oscillator. | R/W | 1 |
| 3 | RCOSCEN | It decides oscillation of the 32kHz RC oscillator. Output clock of the 32kHz RC | R/W | 1 |

| | | | | |
|---|---|---|---|---|
| | | oscillator is used for sleep timer and the watchdog timer.<br>1: Enables the 32kHz RC oscillator.<br>0: Disables the 32kHz RC oscillator. | | |
| 2 | SELRTCLK | It selects sleep timer clock source.<br>When this field is set to 0, output clock of the 32kHz RC oscillator is used as a clock source. Optionally, the external 32.768kHz crystal oscillator is used as a clock source of the sleep timer and watchdog timer by setting to 1 | R/W | 0 |
| 1:0 | PDMODE | Register for power down mode of MG2471<br>00: Normal operation mode<br>01: PM1<br>10: PM2<br>11: PM3 | R/W | 00 |

**RCOSC (RC OSCILLATOR CALIBRATION REGISTER, 0x22E1)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | - | Reserved | RO | 1 |
| 6 | HSRCCEN | It enables or disables calibration block in the 16MHz RC oscillator.<br>1: Enables 16MHz RC Calibration.<br>0: Disables 16MHz RC Calibration. | R/W | 0 |
| 5 | HSRCCRSTB | | R/W | 0 |
| 4 | - | Reserved | RO | 1 |
| 3 | RCCEN | It enables or disables calibration block in the 32kHz RC oscillator.<br>1: Enables 32kHz RC Calibration.<br>0: Disables 32kHz RC Calibration. | R/W | 1 |
| 2 | RCCRSTB | | RO | 0 |
| 1 | | Reserved | RO | 0 |
| 0 | | Reserved. | RO | 0 |

**RTINT1 (SLEEP TIMER INTERVAL CONTROL REGISTER, 0x22E3)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | RTVALSEC[15:8] | This field determines the Sleep timer interval with RTINT2, RTINT3, and EXPRTVAL bits in PDMON. | R/W | 0x00 |

**RTINT2 (SLEEP TIMER INTERVAL CONTROL REGISTER, 0x22E4)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | RTVALSEC[7:0] | This field determines the Sleep timer interval with RTINT1, RTINT3, and EXPRTVAL bits in PDMON. | R/W | 0x01 |

### RTINT3 (SLEEP TIMER INTERVAL CONTROL REGISTER, 0x22E5)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | RTVALSUB[7:0] | This field determines the Sleep timer interval with RTINT1, RTINT2, and EXPRTVAL bits in PDMON. | R/W | 0x00 |

### PDMON (RC OSCILLATOR CALIBRATION REGISTER, 0x22E6)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | RTCPRDSEL | This field determines step of the Sleep timer interval<br>0: 30.5usec<br>1: 3.904msec | R/W | 1 |
| 6 | OSCOK | 32MHz crystal oscillator status:<br>0: 32MHz crystal oscillator is not yet stable.<br>1: 32MHz crystal oscillator is stable. | RO | 0 |
| 5 | | Reserved | RO | 0 |
| 4:3 | EXPRTVAL | This field determines the Sleep timer interval with RTINT1, RTINT2, and RTINT3. | R/W | 0 |
| 2 | ACHMEN | It enables or disables ADC input MUX.<br>1: Enables ADC input MUX.<br>0: Disables ADC input MUX. (ACH0-ACH3 pins are floated) | R/W | 1 |
| 1:0 | | Reserved | RO | 0x3 |

### GPIOPS0 (PORT 0, PULL-UP/PULL-DOWN SELECT REGISTER, 0x22E7)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | GPIO0_PS | This field selects the configuration of Port 0 as pull-up/pull-down inputs<br>0: pull-down<br>1: pull-up | R/W | 0xFF |

### GPIOPS1 (PORT 1, PULL-UP/PULL-DOWN SELECT REGISTER, 0x22E8)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | GPIO1_PS | This field selects the configuration of Port 1 as pull-up/pull-down inputs<br>0: pull-down<br>1: pull-up | R/W | 0xFF |

### GPIOPS3 (PORT 3, PULL-UP/PULL-DOWN SELECT REGISTER, 0x22E9)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | GPIO3_PS | This field selects the configuration of Port 3 as pull-up/pull-down inputs<br>0: pull-down<br>1: pull-up | R/W | 0xFF |

### GPIOPE0 (PORT 0, INPUT MODE, 0x22EA)

| Bit | Name | Descriptions | R/W | Reset |
|---|---|---|---|---|

| Field | | | | Value |
|---|---|---|---|---|
| 7:0 | GPIO0_PE | This field selects input mode of the Port 0.<br>0: tri-state<br>1: pull-up/pull-down ( see GPIOPS0(0x22E7)) | R/W | 0xFF |

**GPIOPE1 (PORT 1, INPUT MODE, 0x22EB)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | GPIO1_PE | This field selects input mode of the Port 1.<br>0: tri-state<br>1:pull-up/pull-down(see PIOPS0(0x22E8)) | R/W | 0xFF |

**GPIOPE3 (PORT 3, INPUT MODE, 0x22EC)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | GPIO3_PE | This field selects input mode of the Port 3.<br>0: tri-state<br>1:pull-up/pull-down(see PIOPS0(0x22E9)) | R/W | 0xFF |

**GPIOPOL0 (PORT 0, INTERRUPT POLARITY, 0x22ED)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | GPIO0_POLH | This field changes the polarity of the Port 0. Port 0 is used the wake up source in the PM1/2/3<br>0: recognizes low level as interrupt signal.<br>1: recognizes high level as interrupt signal. | R/W | 0x00 |

**GPIOPOL1 (PORT 1, INTERRUPT POLARITY, 0x22EE)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | GPIO1_POLH | This field changes the polarity of the Port 1. Port 1 is used the wake up source in the PM1/2/3<br>0: recognizes low level as interrupt signal.<br>1: recognizes high level as interrupt signal. | R/W | 0x00 |

**GPIOPOL3 (PORT 3, INTERRUPT POLARITY, 0x22EF)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | GPIO3_POLH | This field changes the polarity of the Port 3. Port 3 is used the wake up source in the PM1/2/3<br>0: recognizes low level as interrupt signal.<br>1: recognizes high level as interrupt signal. | R/W | 0x00 |

**GPIOMSK0 (PORT 0, INTERRUPT MASK, 0x22F0)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | GPIO0_MSK | Port 0 interrupt mask. Port 0 is used the wake up source when this field is set to 1 in PM1/2/3.<br>0: No interrupt will be acknowledged.<br>1: Port 0 is individually enabled and Port 0 is used the wake up source. | R/W | 0x00 |

**GPIOMSK1 (PORT 1, INTERRUPT MASK, 0x22F1)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | GPIO1_MSK | Port 1 interrupt mask. Port 1 is used the wake up source when this field is set to 1 in PM1/2/3. | R/W | 0x00 |

| | | | | |
|---|---|---|---|---|
| | | 0: No interrupt will be acknowledged.<br>1: Port 1 is individually enabled and Port 1 is used the wake up source. | | |

**GPIOMSK3 (PORT 3, INTERRUPT MASK, 0x22F2)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0, | GPIO3_MSK | Port 3 interrupt mask. Port 3 is used the wake up source when this field is set to 1 in PM1/2/3.<br>0: No interrupt will be acknowledged.<br>1: Port 3 is individually enabled and Port 3 is used the wake up source. | R/W | 0x0C |

# 9. TRANSCEIVER

## 9.1. MAC

The MAC block transmits the data received from high layer to baseband modem, or encrypts it and then transmits to baseband modem. In addition, it indicates the status of PHY and transmits the data received from baseband modem to high layer, or transmits the decrypted data to high layer.

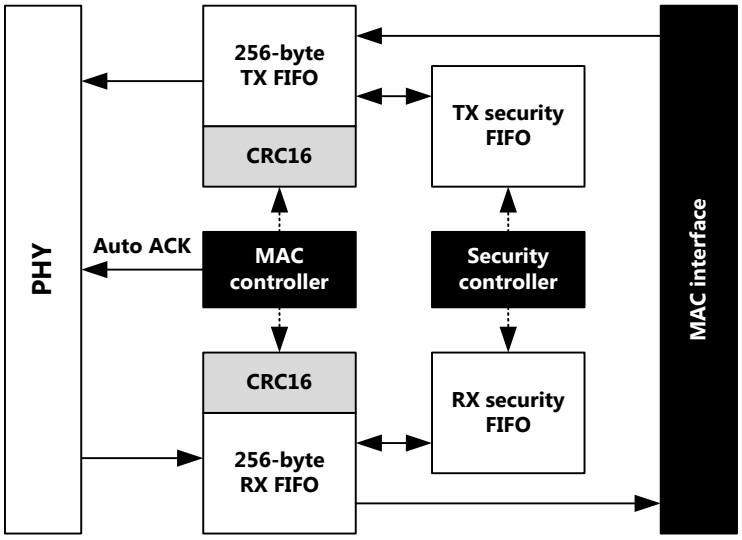



**Figure 19. MAC block diagram**

[Figure 19] shows the MAC block structure. The RX and TX FIFOs are separately implemented. The size of each FIFO is 256 bytes in order to process one IEEE802.15.4 packet along with buffering one packet. The MAC FIFO and security FIFO shares the address space and are distinguished by setting the register of SECMAP (0x219F). The following table shows the address space of each FIFO.

**MTXFIFO or STXFIFO (MAC TX FIFO or SECURITY TX FIFO, 0x2300~0x23FF)**

| Name | Descriptions | R/W | Reset Value |
|---|---|---|---|
| MTXFIFO or STXFIFO | Random access space for MAC TX FIFO (MTXFIFO; SECMAP = 0)<br>or security TX FIFO (STXFIFO; SECMAP = 1) | R/W | 0x00 |

**MRXFIFO or SRXFIFO (MAC RX FIFO or SECURITY RX FIFO, 0x2400~0x24FF)**

| Name | Descriptions | R/W | Reset Value |
|---|---|---|---|
| MRXFIFO or SRXFIFO | Random access space for MAC RX FIFO (MRXFIFO; SECMAP = 0)<br>or RX security FIFO (SRXFIFO; SECMAP = 1) | R/W | 0x00 |

The general MAC/security control registers except for FIFO control registers are prepared as following.

**KEY0 (ENCRYPTION KEY 0 REGISTER, 0x2100~0x210F)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 127:0 | KEY0 | 16-byte key (KEY0) for AES-128<br>0x210F: Most significant byte | R/W | 0 |

**RXNONCE (RX NONCE FOR AUTHENTICATION REGISTER, 0x2110~0x211C)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 103:0 | RXNONCE | Used for decryption: 8-byte source address + 4-byte frame counter + 1-byte key sequence counter<br>0x211C: Most significant byte of source address<br>0x2114: Most significant byte of frame counter<br>0x2110: Key sequence counter | R/W | 0 |

**KEY1 (ENCRYPTION KEY 1 REGISTER, 0x2130~0x213F)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 127:0 | KEY1 | 16-byte key (KEY1) for AES-128<br>0x213F: Most significant byte | R/W | 0 |

**TXNONCE (TX NONCE FOR AUTHENTICATION REGISTER, 0x2140~0x214C)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 103:0 | TXNONCE | Used for encryption: 8-byte source address + 4-byte frame counter + 1-byte key sequence counter<br>0x214C: Most significant byte of source address<br>0x2144: Most significant byte of frame counter<br>0x2140: Key sequence counter | R/W | 0 |

**EXTADDR (EXTENDED ADDRESS REGISTER, 0x2150~0x2157)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 63:0 | EXTADDR | 64-bit IEEE address<br>0x2157: Most significant byte | R/W | 0 |

**PANID (PAN IDENTIFIER REGISTER, 0x2158~0x2159)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 15:0 | PANID | 16-bit PAN ID<br>0x2159: Most significant byte | R/W | 0 |

**SHORTADDR (SHORT ADDRESS REGISTER, 0x215A~0x215B)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 15:0 | SHORTADDR | 16-bit short (network) address<br>0x215B: Most significant byte | R/W | 0 |

**MACSTS (MAC/SECURITY STATUS REGISTER, 0x2180)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | ENCDEC | When this field is set to ’1’, there is data in the encryption or decryption. | RO | 0 |
| 6 | TX_BUSY | When this field is set to ’1’, data in the TX FIFO is transmitted to a modem. | RO | 0 |

| | | | | |
|---|---|---|---|---|
| 5 | RX_BUSY | When this field is set to ‘1’, data is transmitted from a modem to the RX FIFO. | RO | 0 |
| 4 | | Reserved | | |
| 3 | DECODE_OK | This field checks the validity of data according to the type of data received or the address mode.<br>If there is no problem, this field is set to ‘1’ | RO | 0 |
| 2 | ENC_DONE | When encryption operation is finished, this field is set to ‘1’. | R/W | 0 |
| 1 | DEC_DONE | When decryption operation is finished, this field is set to ‘1’. | R/W | 0 |
| 0 | CRC_OK | If there is no problem for checking CRC of received packet, this field is set to ‘1’. | R/W | 0 |

**MACRST (MAC/SECURITY RESET REGISTER, 0x2190)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | RST_FIFO | When this field is set to ‘1’, the MAC FIFO is initialized. | R/W | 0 |
| 6 | RST_TSM | When this field is set to ‘1’, the MAC TX state machine is initialized. | R/W | 0 |
| 5 | RST_RSM | When this field is set to ’1’, the MAC RX state machine is initialized. | R/W | 0 |
| 4 | RST_AES | When this field is set to ‘1’, the AES engine is initialized. | R/W | 0 |
| 3:0 | | Reserved | | 0x0 |

**MACCTRL (MAC CONTROL REGISTER, 0x2191)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:5 | | Reserved | RO | 0 |
| 4 | PREVENT_ACK | When this field is set to ‘1’, the RX interrupt doesn’t occur when the DSN field of received ACK packet is different from the value in MACDSN register during packet reception. | R/W | 0 |
| 3 | PAN_COORDINATOR | When this field is set to ‘1’, function for PAN coordinator is enabled. | R/W | 0 |
| 2 | ADR_DECODE | When this field is set to ‘1’, the RX interrupt doesn’t occur when address information of the received packet is not matched with device itself. | R/W | 0 |
| 1 | AUTO_CRC | When this field is set to ‘1’, the RX interrupt doesn’t occur when the CRC of the received packet is not valid. | R/W | |
| 0 | | Reserved | RO | 0 |

**MACDSN (MAC DSN, 0x2192)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | MACDSN | If the DSN field of the received ACK packet is not equal to MACDSN, the RX interrupt does not occurred. | R/W | 0 |

### SECCTRL (SECURITY CONTROL REGISTER, 0x2193)

<table>
<tr><th>Bit Field</th><th>Name</th><th>Descriptions</th><th>R/W</th><th>Reset Value</th></tr>
<tr><td>7</td><td>SA_KEYSEL</td><td>Selects the KEY value for standalone SAES operation. When this field is ‘1’, KEY1 is selected and when ‘0’, KEY0 is selected.</td><td>R/W</td><td>0</td></tr>
<tr><td>6</td><td>TX_KEYSEL</td><td>Selects the KEY value for AES operation during packet transmission. When this field is ’1’, KEY1 is selected and when ‘0’, KEY0 is selected.</td><td>R/W</td><td>0</td></tr>
<tr><td>5</td><td>RX_KEYSEL</td><td>Selects the KEY value for AES operation when packet reception. When this field is ‘1’, KEY1 is selected and when ‘0’, KEY0 is selected.</td><td>R/W</td><td>0</td></tr>
<tr><td>4:2</td><td>SEC_M</td><td>In CBC-MAC operation, it represents the data length used in the authentication field in byte.<br><table><tr><th>SEC_M</th><th>Authentication field length</th></tr><tr><td>1</td><td>4</td></tr><tr><td>2</td><td>6</td></tr><tr><td>3</td><td>8</td></tr><tr><td>4</td><td>10</td></tr><tr><td>5</td><td>12</td></tr><tr><td>6</td><td>14</td></tr><tr><td>7</td><td>16</td></tr></table></td><td>R/W</td><td>0x0</td></tr>
<tr><td>1:0</td><td>SEC_MODE</td><td>Security mode.<br>0x0: No security<br>0x1: CBC-MAC mode<br>0x2: CTR mode<br>0x3: CCM mode</td><td>R/W</td><td>0x0</td></tr>
</table>

### TXL (AES OPERATION LENGTH FOR TRANSMIT PACKET REGISTER, 0x2194)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | | Reserved | RO | 0 |
| 6:0 | TXL | This field represents the length used in the AES operation for the packet to be transmitted. It has a different meaning for each security mode as follows.<br><br>Security mode: CTR<br>It represents the number of bytes between length byte and the data to be encrypted or decrypted of data in FIFO.<br><br>Security mode: CBC-MAC<br>It represents the number of byte between length byte and the data to be authenticated.<br><br>Security mode: CCM<br>It represents the length of data which is used not in encoding or decoding but in authentication. | R/W | 0x00 |

**RXL (AES OPERATION LENGTH FOR RECEIVED PACKET REGISTER, 0x2195)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | | Reserved | RO | 0 |
| 6:0 | RXL | This field represents the length used in the AES operation for the received packet and it has a different meaning for each security mode as follows.<br><br>Security mode: CTR<br>It represents the number of bytes between length byte and the data to be encrypted or decrypted of data in FIFO.<br><br>Security mode: CBC-MAC<br>It represents the number of bytes between length byte and the data to be authenticated.<br><br>Security mode: CCM<br>It represents the length of data which is used not in encoding or decoding but in authentication. | R/W | 0x00 |

**SECMAP (MAC/SECURITY REGISTER MAP SELECTION REGISTER, 0x219F)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:1 | | Reserved | RO | 0 |
| 0 | SECMAP | MAC/security control/FIFO register map selection<br>0x0: MAC control / MAC FIFO selected<br>0x1: Security control / security FIFO selected | R/W | 0 |

### 9.1.1. Receive Mode

When receiving the data from the PHY block, the MAC block stores the data in the RX FIFO. The data in the RX FIFO can be read by the MRFCPOP (0x2080) register. Data decryption is implemented by AES-128 algorithm, which supports CCM* mode by ZigBee and CTR/CBC-MAC/CCM mode by IEEE 802.15.4. The RX Controller controls the process described above. When decrypting the data, the received frame data length is modified and the modified value is stored in the LSB of each frame by the hardware again.

The size of the RX FIFO is 256 bytes and it is implemented by a circular FIFO with a write pointer and a read pointer. The RX FIFO can store several frame data received from the PHY block. Since the LSB of each frame data represents the frame data length, it can be accessed by the write pointer and the read pointer.

When the data is received from the PHY block, the CRC information is checked to verify data integrity.
When AUTO_CRC control bit of MACCTRL (0x2191) register is set to ‘1’, CRC information is verified by the RX CRC block automatically. To check the result, refer to the CRC_OK field of MACSTS (0x2180) register. When the value of CRC_OK field is set to ‘1’, there is no problem with CRC information. When the AUTO_CRC control bit of the MACCTRL (0x2191) register is not set to ‘1’, the CRC information should be verified by the software.

When a packet reception is completed in the PHY block, a PHY interrupt is sent to the MCU. In addition, when decryption operation is completed, an AES interrupt is sent to the MCU.

The following tables show the MAC RX FIFO control registers. Register address space is shared with the security-related register address space. Therefore, the MAC RX FIFO control registers are accessible when SECMAP is 0x0.

**MRFCPOP (MAC RX FIFO POP REGISTER, 0x2080)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | MRFCPOP | Through this register, data in RX FIFO is read. | RO | |

**MRFCWP (MAC RX FIFO WRITE POINTER REGISTER, 0x2081)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | MRFCWP | RX FIFO write pointer<br>Total size of the write pointer is 9-bit with MRFCWP8 in MRFCSTS register. It is increased by '1' whenever data is written to the RX FIFO. | R/W | 0x00 |

**MRFCRP (MAC RX FIFO READ POINTER REGISTER, 0x2082)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | MRFCRP | RX FIFO read pointer<br>Total size of the read pointer is 9-bit with MRFCRP8 bit in MRFCSTS register. It is increased by '1' whenever data is read from the RX FIFO. | R/W | 0x00 |

**MRFCCTRL (MAC RX FIFO CONTROL REGISTER, 0x2083)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:3 | | Reserved | RO | 0 |
| 2 | ASA | When this field is set to '1', it automatically sets the starting address of a packet and the length of a packet decrypted by the AES engine to the information of the received packet. | R/W | 1 |
| 1 | ENA | When this field is set to '1', RX FIFO is enabled. | R/W | 1 |
| 0 | CLR | When this field is set to '1', MRFCWP, MRFCRP, MRFCSTS, MRFCSIZE registers are initialized. | R/W | 0 |

**MRFCSTS (MAC RX FIFO STATUS REGISTER, 0x2084)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | MRFCWP8 | Total size of the write pointer is 9-bit address with MRFCWP. This field is MSB, and is used to detect wraparound of a circular FIFO.<br>When MRFCWP8 is manually modified, it should be update along with MRFCWP. | R/W | 0 |
| 6 | MRFCRP8 | Total size of the read pointer is 9-bit address with MRFCRP. This field is MSB, and is used to detect wraparound of a circular FIFO.<br>When MRFCRP8 is manually modified, it should be update along with MRFCRP. | R/W | 0 |
| 5:2 | | Reserved | RO | 0 |
| 1 | FULL | RX FIFO full<br>This field is set to '1' when data size in RX FIFO is 256 byte. | RO | 0 |
| 0 | EMPTY | RX FIFO empty | RO | 0 |

| | | | | |
|---|---|---|---|---|
| | | This field is set to '1' when data size in RX FIFO is '0'. | | |

**MRFCSIZE (NUMBER OF DATA IN MAC RX FIFO REGISTER, 0x2085)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | MRFCSIZE | This field represents the number of valid data bytes of RX FIFO. This field value is valid when the FIFO status is normal and is calculated by the difference between MRFCWP and MRFCRP. | R/W | 0x00 |

### 9.1.2. Transmit Mode

To transmit the data from a higher layer (MCU) to the PHY block, the device stores the data in the TX FIFO of the MAC block. When the MCU writes data in the MTFCPUSH (0x2000) register, data is stored in TX FIFO of MAC. The size of the TX FIFO is 256 byte and it is implemented by a circular FIFO with a write pointer and a read pointer. Since each data in TX FIFO is mapped to the memory area in the MCU, it can be written or read directly by the MCU.

The data stored in the TX FIFO can be transmitted to the PHY block by the TX request command of PCMD0 (0x2200) register. The TX controller controls the process described above. Data encryption is implemented by the AES-128 algorithm, which supports CCM* mode by ZigBee and CTR/CBC-MAC/CCM mode by IEEE 802.15.4. The data length which is to be transmitted is stored in the LSB of each frame by the software when the frame data is stored in TX FIFO by the MCU. When the data in TX FIFO is encrypted, the data length is modified and then stored by the hardware again.

When transmitting the data in the TX FIFO, the CRC operation is processed to verify data integrity. When the AUTO_CRC control bit of the MACCTRL (0x2191) register is set to '1', CRC information is generated by TX CRC block automatically. Otherwise, CRC operation should be operated by software.

When data encryption is completed, an AES interrupt is sent to the MCU. When the data transmission to the PHY block is completed, a PHY interrupt is sent to the MCU.

The following tables show the MAC TX FIFO control registers. Register address space is shared with the security-related register address space. Therefore, the MAC TX FIFO control registers are accessible when SECMAP is 0x0.

**MTFCPUSH (MAC TX FIFO PUSH REGISTER, 0x2000)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | MTFCPUSH | When data is written to this register, it is stored in TX FIFO. | WO | |

**MTFCWP (MAC TX FIFO WRITE POINTER REGISTER, 0x2001)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | MTFCWP | TX FIFO write pointer<br>Total size of the write pointer is 9-bit with MTFCWP8 in MTFCSTS register. It is increased by '1' whenever data is written to the TX FIFO. | R/W | 0x00 |

**MTFCRP (MAC TX FIFO READ POINTER REGISTER, 0x2002)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | MTFCRP | TX FIFO read pointer<br>Total size of the read pointer is 9-bit with MTFCRP8 bit in MTFCSTS register. It is increased by '1' whenever data is read from the TX FIFO. | R/W | 0x00 |

**MTFCCTRL (MAC TX FIFO CONTROL REGISTER, 0x2003)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:3 | | Reserved | RO | 0 |
| 2 | ASA | When this field is set to '1', it automatically sets the starting address of a packet and the length of a packet encrypted by the AES engine to the information of the packet which is to be transmitted. | R/W | 1 |
| 1 | ENA | When this field is set to '1', TX FIFO is enabled | R/W | 1 |
| 0 | CLR | When this field is set to '1', the MTFCWP, MTFCRP, MTFCSTS, MTFCSIZE registers are initialized. | R/W | 0 |

**MTFCSTS (MAC TX FIFO STATUS REGISTER, 0x2004)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | MTFCWP8 | Total size of the write pointer is 9-bit address with MTFCWP. This field is MSB, and is used to detect wraparound of a circular FIFO.<br>When MTFCWP8 is manually modified, it should be update along with MTFCWP. | R/W | 0 |
| 6 | MTFCRP8 | Total size of the read pointer is 9-bit address with MTFCRP. This field is MSB, and is used to detect wraparound of a circular FIFO.<br>When MTFCRP8 is manually modified, it should be update along with MTFCRP. | R/W | 0 |
| 5:2 | | Reserved | RO | 0 |
| 1 | FULL | TX FIFO full<br>This field is set to '1' when data size in TX FIFO is 256 byte. | RO | 0 |
| 0 | EMPTY | TX FIFO empty<br>This field is set to '1' when data size in TX FIFO is '0'. | RO | 0 |

**MTFCSIZE (NUMBER OF DATA IN MAC TX FIFO REGISTER, 0x2005)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | MTFCSIZE | This field represents the number of valid data bytes of TX FIFO. This field value is valid when the FIFO status is normal and is calculated by the difference between MTFCWP and MTFCRP. | R/W | 0x00 |

### 9.1.3. Data Encryption and Decryption

Data encryption or decryption is done by the security controller block. Security Controller consists of the block for processing encryption/decryption operation and the block for controlling.

In order to implement CCM* mode by ZigBee and CTR/CBC-MAC/CCM mode by IEEE 802.15.4, 128-bit key value and a nonce are needed. MG2471 can have two 128-bit key values, KEY0 and KEY1. For encryption, the desired nonce value should be stored in the TX Nonce and KEY0 or KEY1 should be selected for use. For decryption, the desired nonce value should be stored in the RX Nonce and KEY0 or KEY1 should be selected for use. For more detailed information, refer to the IEEE802.15.4 standard document.

The following registers describe the security TX/RX FIFO control registers. They are accessible when SECMAP is 0x1.

**STFCPUSH (SECURITY TX FIFO PUSH REGISTER, 0x2000)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | STFCPUSH | When data is written to this register, it is stored in security TX FIFO. | WO | |

**STFCWP (SECURITY TX FIFO WRITE POINTER REGISTER, 0x2001)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | STFCWP | Security TX FIFO write pointer<br>Total size of the write pointer is 9-bit with STFCWP8 in STFCSTS register. It is increased by '1' whenever data is written to the security TX FIFO. | R/W | 0x00 |

**STFCRP (SECURITY TX FIFO READ POINTER REGISTER, 0x2002)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | STFCRP | Security TX FIFO read pointer<br>Total size of the read pointer is 9-bit with STFCRP8 in STFCSTS register. It is increased by '1' whenever data is read from the security TX FIFO. | R/W | 0x00 |

**STFCCTRL (SECURITY TX FIFO CONTROL REGISTER, 0x2003)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:2 | | Reserved | RO | 0 |
| 1 | ENA | When this field is set to '1', security TX FIFO is enabled. | R/W | 1 |
| 0 | CLR | When this field is set to '1', STFCWP, STFCRP, STFCSTS, STFCSIZE registers are initialized. | R/W | 0 |

**STFCSTS (SECURITY TX FIFO STATUS REGISTER, 0x2004)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | STFCWP8 | Total size of the write pointer is 9-bit address with STFCWP. This field is MSB, and is used to detect wrap around of a circular FIFO. | R/W | 0 |
| 6 | STFCRP8 | Total size of the read pointer is 9-bit address with STFCRP. This field is MSB, and is used to detect wrap around of a circular FIFO. | R/W | 0 |
| 5:2 | | Reserved | RO | 0 |
| 1 | FULL | Security TX FIFO full<br>This field is set to '1' when data size in | RO | 0 |

| | | | | |
|---|---|---|---|---|
| | | security TX FIFO is 256 byte. | | |
| 0 | EMPTY | Security TX FIFO empty<br>This field is set to '1' when data size in security TX FIFO is '0'. | RO | 0 |

**STFCSIZE (NUMBER OF DATA IN SECURITY TX FIFO REGISTER, 0x2005)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | STFCSIZE | This field represents the number of valid data bytes of security TX FIFO. This field value is valid when the FIFO status is normal and is calculated by the difference between STFCWP and STFCRP. | R/W | 0x00 |

**STFCSECBASE (ENCRYPTION FRAME BASE ADDRESS REGISTER, 0x2007)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | STFCSECBASE | Frame base address for encryption | R/W | 0x00 |

**STFCSECLEN (ENCRYPTION FRAME LENGTH REGISTER, 0x2008)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | STFCSECLEN | Frame length for encryption | R/W | 0x00 |

**STFDMALEN (DIRECT DATA TRANSFER SIZE REGISTER, 0x2009)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | STFDMALEN | Data size of direct transfer between the security TX FIFO and the TX FIFO. | R/W | 0x00 |

**STFDMACTRL (DIRECT DATA TRANSFER CONTROL REGISTER, 0x200A)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:2 | | Reserved | RO | 0 |
| 1 | BUSY | When this field is set to '1', data transfer between the TX security FIFO and the TX FIFO is activated. | RO | 0 |
| 0 | ENA | Enable the direct transfer between the security TX FIFO and the TX FIFO | WO | 0 |

**SRFCPOP (SECURITY RX FIFO POP REGISTER, 0x2080)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | SRFCPOP | Through this register, data in security RX FIFO is read. | WO | |

**SRFCWP (SECURITY RX FIFO WRITE POINTER REGISTER, 0x2081)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | SRFCWP | Security RX FIFO write pointer<br>Total size of the write pointer is 9-bit with SRFCWP8 in SRFCSTS register. It is increased by '1' whenever data is written to the security RX FIFO. | R/W | 0x00 |

### SRFCRP (SECURITY RX FIFO READ POINTER REGISTER, 0x2082)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | SRFCRP | Security RX FIFO read pointer<br>Total size of the read pointer is 9-bit with SRFCRP8 in SRFCSTS register. It is increased by '1' whenever data is read from the security RX FIFO. | R/W | 0x00 |

### SRFCCTRL (SECURITY RX FIFO CONTROL REGISTER, 0x2083)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:2 | | Reserved | RO | 0 |
| 1 | ENA | When this field is set to '1', security RX FIFO is enabled. | R/W | 1 |
| 0 | CLR | When this field is set to '1', SRFCWP, SRFCRP, SRFCSTS, SRFCSIZE registers are initialized. | R/W | 0 |

### SRFCSTS (SECURITY RX FIFO STATUS REGISTER, 0x2084)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7 | SRFCWP8 | Total size of the write pointer is 9-bit address with SRFCWP. This field is MSB, and is used to detect wrap around of a circular FIFO. | R/W | 0 |
| 6 | SRFCRP8 | Total size of the read pointer is 9-bit address with SRFCRP. This field is MSB, and is used to detect wrap around of a circular FIFO. | R/W | 0 |
| 5:2 | | Reserved | RO | 0 |
| 1 | FULL | Security RX FIFO full<br>This field is set to '1' when data size in security RX FIFO is 256 byte. | RO | 0 |
| 0 | EMPTY | Security RX FIFO empty<br>This field is set to '1' when data size in security RX FIFO is '0'. | RO | 0 |

### SRFCSIZE (NUMBER OF DATA IN SECURITY RX FIFO REGISTER, 0x2085)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | SRFCSIZE | This field represents the number of valid data bytes of security RX FIFO. This field value is valid when the FIFO status is normal and is calculated by the difference between SRFCWP and SRFCRP. | R/W | 0x00 |

### SRFCSECBASE (DECRYPTION FRAME BASE ADDRESS REGISTER, 0x2087)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | SRFCSECBASE | Frame base address for decryption | R/W | 0x00 |

### SRFCSECLEN (DECRYPTION FRAME LENGTH REGISTER, 0x2088)

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | SRFCSECLEN | Frame length for decryption | R/W | 0x00 |

**SRFDMALEN (DIRECT DATA TRANSFER SIZE REGISTER, 0x2089)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:0 | SRFDMALEN | Data size of direct transfer between the security RX FIFO and the RX FIFO. | R/W | 0x00 |

**SRFDMACTRL (DIRECT DATA TRANSFER CONTROL REGISTER, 0x208A)**

| Bit Field | Name | Descriptions | R/W | Reset Value |
|---|---|---|---|---|
| 7:2 | | Reserved | RO | 0 |
| 1 | BUSY | When this field is set to '1', data transfer between the security RX FIFO and the RX FIFO is activated. | RO | 0 |
| 0 | ENA | Enable the direct transfer between the security RX FIFO and the RX FIFO | WO | 0 |

## 9.2. PHY

The baseband PHY (a.k.a. modem) is composed of the O-QPSK modulator and demodulator with simple convolutional channel coder. [Figure 19] shows the baseband PHY structure.

The modulation starts from fetching the data in the TX MAC FIFO. The PHY payload (PHY service data unit; PSDU) can be optionally encoded with the convolutional channel encoder. After appending the preamble, SFD and length field to the PHY payload, a constructed frame (PHY protocol data unit; PPDU) is mapped to designated symbols according to the data-rate control of the PHY controller. Each symbol is accordingly spread by the DSSS chip modulator. The spread PHY bit stream in the chip-level is then modulated to the O-QPSK signal and transmitted by the RF transmitter. For the 250Kbps data-rate packet, its structure is fully compatible with the IEEE802.15.4 O-QPSK PHY specification.

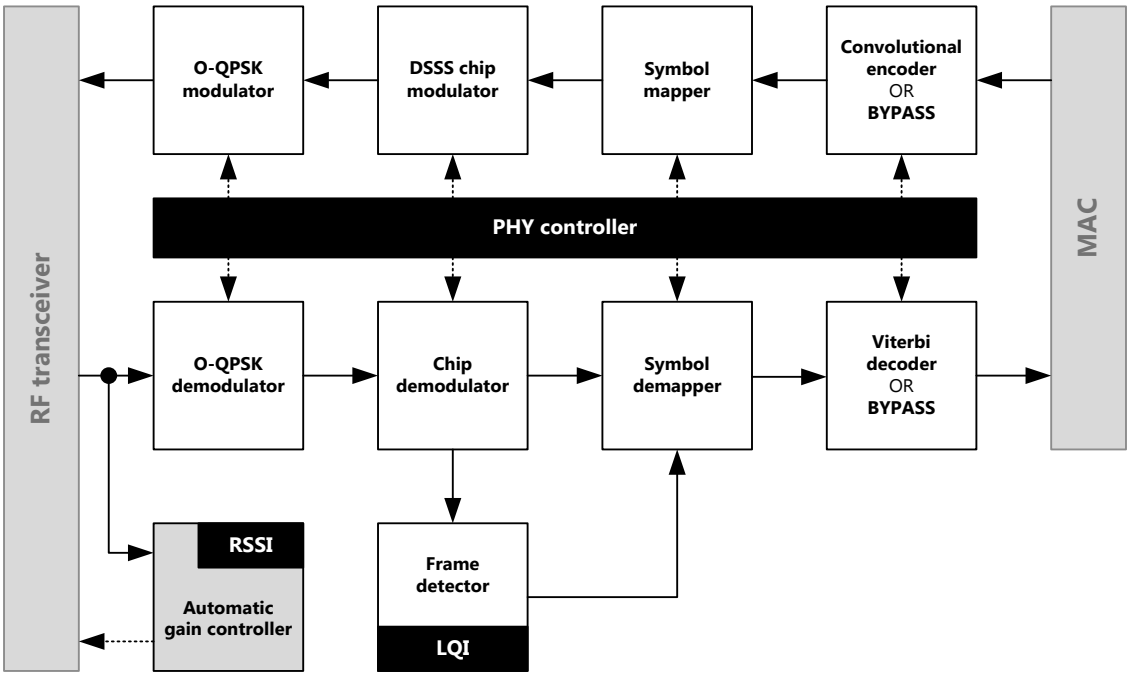



**Figure 20. Baseband PHY**

With the RF receiver, the received O-QPSK signal is demodulated to the chip sequences. The gain amplifying blocks in the RF receiver are controlled by the automatic gain controller (AGC). The chip sequence is appropriately de-spread by the chip demodulator, and then the start of the designated frame is determined by detecting the synchronization header (preamble and SFD). When the SFD is detected, the baseband PHY generates the interrupt which indicates the start of a packet.

The length and the PHY payload followed by the synchronization header are decoded by the symbol demapper and Viterbi decoder (if the convolutional encoding is applied), and stored in the RX MAC FIFO. When the last data of the PHY payload is stored, the interrupt is generated to indicate the end of the packet reception. After a packet reception interrupt occurs, the RX MAC procedure is performed.

When a packet is received, the baseband PHY provides both of the received signal strength Indicator (RSSI) and the link quality indicator (LQI). They can be used to decide the quality of the communication channel.

While a packet does not exist, the baseband PHY continuously provides the RF channel energy level at antenna. The measured energy level is used to decide the communication channel state. Clear channel assessment (CCA) operation is based on this information. The CCA operation is used to prevent a collision when multiple users try to use a channel simultaneously. When a channel is determined to be busy, packet transmission is deferred until the channel state changes to idle.

### 9.2.1. Interrupt

The baseband PHY has 4 interrupt sources to notify the MCU of specific events.

▪ RX END (RXEND_INT)

This interrupt notifies the MCU of the completion of a packet reception. When this interrupt has been generated, the received data in RX MAC FIFO can be handled. Also, the quality of the transmission channel can be checked by reading the RSSI/LQI registers.

▪ RX START (RXSTART_INT)

This interrupt notifies the MCU of the start of a packet reception. (Note: It is not recommended to use RX START Interrupt normally.)

▪ TX END (TXEND_INT)

This interrupt notifies the MCU of the end of a packet transmission. A new packet cannot be transmitted until a packet transmission is completed. When a communication channel is busy, a TX END Interrupt can be delayed until a communication channel goes to the idle state and the transmission is completed successfully.

▪ MODEM READY (MDREADY_INT)

This interrupt notifies the MCU that the state of the baseband PHY has changed from the idle state to the ready state (either RX or TX) for requesting “modem ON”. The baseband PHY is in the idle state when the supply power is turned on, but needs to be changed to the ready state in order to transmit or receive the packet. This interrupt occurs when the RF transceiver has been stabilized by following the “modem ON” request.

▪ MODEM READY FAIL (MDREADYFAIL_INT)

This interrupt notifies the MCU that the modem block has failed to change state from the idle state to the ready state. When the PLL in the RF transceiver is unlocked during dedicated time interval, this interrupt is generated and the state of the baseband PHY remains at the PLL setting state (although it is a transition state as shown in Figure 25).

The interrupt source can be indentified through the INTSTS register. Some interrupt sources can be masked by setting the INTCON register. The baseband PHY also provides the INTIDX register for indicating the interrupt source. The interrupt sources have priority: MDREADY_INT (0) > TXEND_INT (1) > RXSTART_INT (2) > RXEND_INT (3) > MDREADYFAIL_INT (4). The INTIDX register indicates the highest-priority interrupt source among the present interrupts (not cleared). In order to clear the interrupt, it is sufficient to just read the INTIDX register and then the interrupt is cleared (one by one) in priority order.

**INTCLRSEQ (INTERRUPT CLEAR SEQUENCE REGISTER,0x228C)**
This register is used to set the sequence of interrupt clear.

<table>
<tr><th>Bit Field</th><th>Name</th><th>Descriptions</th><th>RW</th><th>Reset Value</th></tr>
<tr><td>[7:5]</td><td>(Reserved)</td><td></td><td>RO</td><td>0</td></tr>
<tr><td>[4:0]</td><td>INTCLRSEQ</td><td>Interrupt clear sequence
<table>
<tr><th>bit</th><th>Description</th></tr>
<tr><td>[0]</td><td>When this field is set to ‘1’, the modem on interrupt is cleared by interrupt clear command.</td></tr>
<tr><td>[1]</td><td>When this field is set to ‘1’, the tx start interrupt is cleared by interrupt clear command.</td></tr>
<tr><td>[2]</td><td>When this field is set to ‘1’, the rx start interrupt is cleared by interrupt clear command.</td></tr>
<tr><td>[3]</td><td>When this field is set to ‘1’, the rx end interrupt is cleared by interrupt clear command.</td></tr>
<tr><td>[4]</td><td>When this field is set to ‘1’, the modem on fail interrupt is cleared by interrupt clear command.</td></tr>
</table></td><td>R/W</td><td>0x00</td></tr>
</table>

**INTCON (PHY INTERRUPT CONTROL REGISTER, 0x228D)**
This register is used to mask off the interrupt of baseband PHY.

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| 7:5 | (Reserved) | | RO | 0 |
| 4 | MDFAILMSK | This field masks MDFAIL_INT off. When MDFAILMSK field is set to ‘0’, MDFAIL_INT interrupt is not generated. | R/W | 0 |
| 3 | RXENDMSK | This field masks RXEND_INT off. When RXENDMSK field is set to ‘0’, RXEND_INT interrupt is not generated. This interrupt should be used to support the successful packet reception. | R/W | 0 |
| 2 | RXSTMSK | This field masks RXEND_START off. When RXSTMSK field is set to ‘0’, RXSTART_INT interrupt is not generated. RXSTART_INT is not a mandatory interrupt. It is recommended to mask off | R/W | 0 |

| | | | | |
|---|---|---|---|---|
| | | RXSTART_INT interrupt when the rapid packet reception is needed. | | |
| 1 | TXENDMSK | This field masks TXEND_INT off. When TXENDMSK field is set to '0', TXEND_INT interrupt is not generated. This interrupt should be used to support the successful packet transmission. | R/W | 0 |
| 0 | MDRDYMSK | This field masks MDRDY_INT off. When MRDYMSK field is set to '0', MDRDY_INT interrupt is not generated. This interrupt should be used to check whether a modem block is ready for transmission /reception or not. | R/W | 0 |

**INTIDX (PHY INTERRUPT STATUS AND INDEX REGISTER, 0x228E)**

This register is used to indicate the kinds of the interrupt when it occurs

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| 7:4 | | (Reserved) | | 0 |
| 3 | ALLINTCLR | This field disables all interrupts when they occur. This field clears all interrupts occurred.<br>When multiple interrupts occur at the same time, the modem block stores them in a buffer and processes them in order. When INTIDX field is read, the executed interrupts are cleared in order. When ALLINTCLR field is set to '0', all the interrupts in buffer are cleared at the same time. | R/W | 1 |
| 2:0 | INTIDX | This register shows the kind of the interrupt when an interrupt occurs, in order if multiple interrupts occur simultaneously. The INTSTS field in the INTSTS register should be used for looking through a list of all interrupts that have been triggered. After reading INTIDX field, executed interrupts are cleared automatically.<br>INTIDX / Interrupt<br>0 MDRDY_INT interrupt<br>1 TXEND_INT interrupt<br>2 RXSTART_INT interrupt<br>3 RXEND_INT interrupt<br>4 MDFAIL_INT interrupt | RO | 0 |

**INTSTS (PHY INTERRUPT STATUS REGISTER, 0x228F)**

This register is used to indicate the kinds of the interrupt when the multiple interrupts occur.

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| 7:5 | | (Reserved) | | 0 |
| 4:0 | INTSTS | Multiple interrupt status<br>This register shows the interrupt status when multiple interrupts occur currently. Each bit in INTSTS field represents the status of a specific interrupt. A table of Bit vs. Interrupt is shown below.<br>Bit / Description<br>0 MDRDY_INT interrupt<br>1 TXEND_INT interrupt<br>2 RXSTART_INT interrupt<br>3 RXEND_INT interrupt<br>4 MDFAIL_INT interrupt | R/W | 0x1F |

| | | | | |
|---|---|---|---|---|
| | | When an interrupt is triggered, the INTSTS field corresponding to each interrupt is set to '0'. To clear the executed interrupt, the bit for each of the executed interrupts should be reset to '1' by software. | | |

### 9.2.2. Data Rate

The MG2471 supports various data rate modes of 31.25Kbps ~ 1Mbps for applications beyond IEEE802.15.4 compliances. The data rate can be selected by using the MDMCNF register (SEL_TXDR and FEC_EN).

The 31.25Kbps ~ 1Mbps modes, which is listed in [Table 9], occupy 2MHz RF channel bandwidth which is the same as the IEEE 802.15.4-2.4GHz 250Kbps standard mode.

The 1Mbps data-rate mode is designed by applying the variable-rate convolutional coding with the same preamble structure as 250Kbps specified in IEEE802.15.4. The other data rate modes are designed by controlling the spreading factor.

**Table 9. Data rate modes**

| Data Rate | FEC_EN | SEL_TXDR | Comment |
|---|---|---|---|
| 1Mbps | 0x1 | 0x0 | |
| 500Kbps | 0x0 | 0x1 | |
| 250Kbps | 0x0 | 0x2 | IEEE802.15.4 compliant |
| 125Kbps | 0x0 | 0x3 | |
| 62.5Kbps | 0x0 | 0x5 | |
| 31.25Kbps | 0x0 | 0x9 | |

### 9.2.3. Forward Error Correction

Especially for higher data rate modes, the MG2471 uses the variable-rate convolutional channel coding for forward error correction (FEC). The MG2471 supports the convolution coding with the rates of 1/2, 2/3, and 3/4.

As shown in [Figure 21], the convolutional encoder with the constraint length of 5 is used for the mother convolutional encoder with the rate of 1/2. $G1(x) = x^4 + x + 1$. $G2(x) = x^4 + x^3 + x^2 + 1$. The rates of 2/3 and 3/4 are available by puncturing of the output of the mother convolutional encoder as shown in [Table 10].

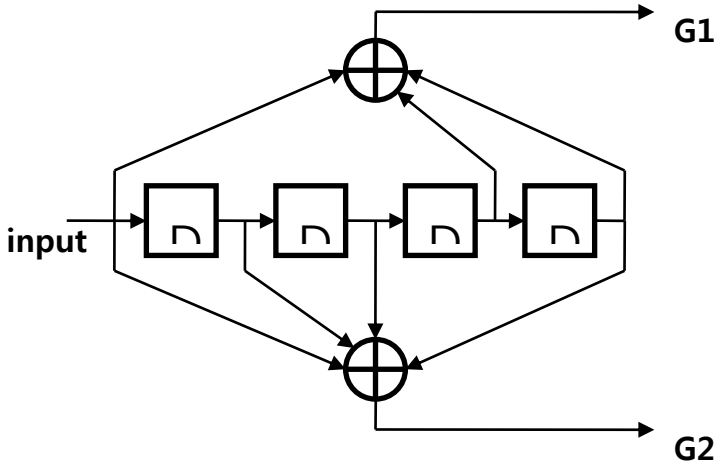



**Figure 21. Convolutional encoder with rate of 1/2**

**Table 10. Puncturing pattern**

| Code rate | Puncturing matrix | Transmitted sequence |
|---|---|---|
| 1/2 | G1: 1<br>G2: 1 | G1[0] G2[0] |
| 2/3 | G1: 1 0<br>G2: 1 1 | G1[0] G2[0] G2[1] |
| 3/4 | G1: 1 0 1<br>G2: 1 1 0 | G1[0] G2[0] G2[1] G1[2] |

### 9.2.4. Packet Format

The MG2471 supports multiple data rates from 31.25Kbps to 1Mbps including 250Kbps specified in IEEE802.15.4. The packet format comparison for high data rates (≥ 250Kbps) with an example payload length of 60-Byte is shown in [Figure 22]. The period of the preamble, SFD, and LEN for 500Kbps, and 1Mbps data-rate modes are the same for 250Kbps mode. Only PHY payload interval is reduced.

The packet format comparison for low data rates (≤250Kbps) with an example payload length of 8-Byte is shown in [Figure 23].

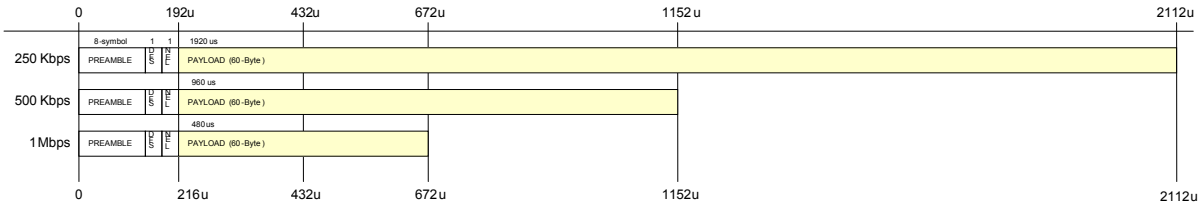



**Figure 22. High data rate packet format**

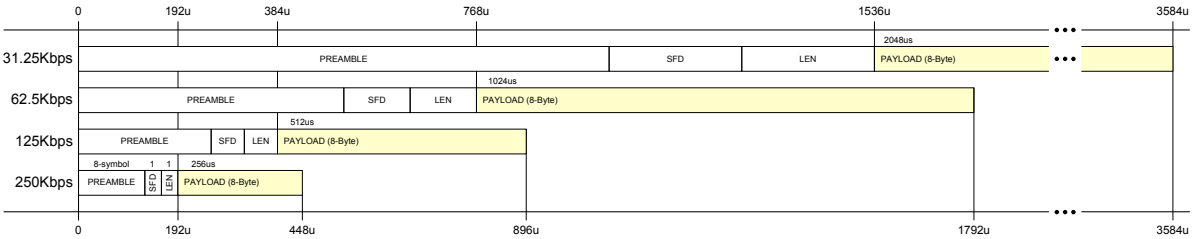



**Figure 23. Low data rate packet format compared to the 250Kbps mode**

**PCMD0 (PHY COMMAND0 REGISTER, 0x2200)**
This register is used to control the operation of baseband PHY.

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| [7:6] | (Reserved) | Only '0' allowed. | R/W | 0 |
| [5] | MODEM_OFF | When this field is set to '0', the baseband PHY status is changed to OFF. In the OFF state, the RF block is in a power-down state and the modem block is in the reset state. In this state, the MG2471 cannot receive or transmit packets. For the transmission or the reception of a packet, the baseband PHY needs to be changed to ON state. When the baseband PHY goes to OFF state, this field is set to '1' automatically by the hardware. | R/W | 1 |
| [4] | MODEM_ON | When this field is set to '0', the baseband PHY status is changed to ON. In ON state,the RF and baseband | R/W | 1 |

| | | | | |
|---|---|---|---|---|
| | | PHY are in the TX or RX ready state. In this state, the modem block controls power-down or power-up for the transmitter or the receiver without an active user application program. When the modem block goes to ON status, this field is set to '1' automatically by the hardware. | | |
| [3] | (Reserved) | Only '1' allowed. | R/W | 1 |
| [2] | TX_REQ | When this field is set to '0', the baseband PHY transmits a packet. When a packet transmission is requested, the baseband PHY changes to the TX ready state. Only when a communication channel is in idle state (CCA= '1'), will the packet be transmitted. When the channel is in busy state (CCA= '0'), the transmission is deferred until the channel state goes to idle. This field is set to '1' automatically by hardware after completing the transmission. When the packet transmission is completed successfully, a TXEND_INT interrupt is sent. If the packet transmission is abnormal, the interrupt in not sent and the TXREQ field is set to '1'. | R/W | 1 |
| [1:0] | (Reserved) | Only '0' allowed. | R/W | 0 |

**PCMD1 (PHY COMMAND1 REGISTER, 0x2201)**

This register is used to control the operation of baseband PHY.

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| [7:2] | (Reserved) | Only '0' allowed. | R/W | 0 |
| [1] | TX_OFF | When this field is set to '1', the TX block is forced to be OFF regardless of the control of the baseband PHY state machine. | R/W | 1 |
| [0] | RX_OFF | When this field is set to '0', the RX block is forced to be OFF regardless of the control of the baseband PHY state machine. | R/W | 1 |

**SETRATE (MODEM DATARATE CONTROL REGISTER, 0x2211)**

This register is used to set data rate and FEC encoding.

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| [7:6] | (Reserved) | Only '0' allowed. | R/W | 0 |
| [5:4] | FEC_EN | Forward error correction encoding :<br>0x0 : UNCODING<br>0x1 : FEC code rate 1/2<br>0x2 : FEC code rate 2/3<br>0x3 : FEC code rate 3/4 | R/W | 0x0 |
| [3:0] | SEL_TXDR[3:0] | Used to select packet data rate | R/W | 0x6 |

| SEL_TXDR | Data Rate |
|---|---|
| 0x0 | 1Mbps (with FEC_EN = 0x1) |
| 0x1 | 500Kbps |
| 0x2 | 250Kbps |
| 0x3 | 125Kbps |
| 0x5 | 62.5Kbps |
| 0x9 | 31.25Kbps |

### 9.2.5. Clear Channel Assessment

While a packet does not exist, the baseband PHY continuously provides the RF channel energy level at antenna. As described before, the measured energy level is used to decide the communication channel state. Clear channel assessment (CCA) operation is based on this information. The CCA operation is used to prevent a collision when multiple users try to use a channel simultaneously. When a channel is determined to be busy, packet transmission is deferred until the channel state changes to idle.

**CCA0 (CLEAR CHANNEL ASSESSMENT0 REGISTER, 0X222C)**
This register is used to set CCA operation environment.

<table>
<tr><th>Bit Field</th><th>Name</th><th>Descriptions</th><th>RW</th><th>Reset Value</th></tr>
<tr><td>[7:6]</td><td>(Reserved)</td><td>Only ‘0’ allowed.</td><td>R/W</td><td>0</td></tr>
<tr><td>[5]</td><td>CCA_FIX</td><td>It fixes the communication channel state to idle. A communication channel state is determined by the CCA circuit in MG2471. When a channel state is busy, a packet is not transmitted. This field allows packet transmission regardless of the channel state. When this field is set to ‘1’, the channel is always in idle state.</td><td>R/W</td><td>1</td></tr>
<tr><td>[4:2]</td><td>CCA_AWS</td><td>This field sets the time duration in which the energy of received signal is measured. It is only valid for the energy detection method.<br><br><table><tr><th>CCA_AWS</th><th>Energy calculation duration</th></tr><tr><td>0</td><td>1 usec</td></tr><tr><td>1</td><td>2 usec</td></tr><tr><td>2</td><td>4 usec</td></tr><tr><td>3</td><td>8 usec</td></tr><tr><td>Others</td><td>16 usec</td></tr></table></td><td>R/W</td><td>0</td></tr>
<tr><td>[1:0]</td><td>CCAMD</td><td>This field sets the method to determine the communication channel state. The following describes the three methods to detect the channel state.<br><br>Energy detection (ED): This method determines the channel state as ‘busy’ when the energy of received signal is higher than the defined level.<br><br>Carrier detection (CD): This method determines the channel state as ‘busy’ when an IEEE802.15.4 carrier is detected.<br><br>Frame detection (FD): This method determines the channel state as ‘busy’ when the normal IEEE802.15.4 packet is detected.<br><br><table><tr><th>CCAMD</th><th>Method</th></tr><tr><td>0</td><td>ED</td></tr><tr><td>1</td><td>CD</td></tr><tr><td>2</td><td>FD</td></tr><tr><td>3</td><td>reserved</td></tr></table></td><td>R/W</td><td>0</td></tr>
</table>

**CCA1 (CLEAR CHANNEL ASSESSMENT1 REGISTER, 0X222D)**
This register is used to set CCA operation environment.

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| [7:0] | CCA1 | This configures the CCA decision threshold when the energy detection method is used as that of the CCA detection. | R/W | 0xB2 |

### 9.2.6. Link Quality Indicator

The MG2471 uses correlation results of multiple symbols in order to calculate an estimate of the LQI value. If LQI_EN is “0x1”, LQI estimation is automatically performed for every received frame except for FEC encoded packets. LQI values are integers ranging from 0 to 255 as required by the IEEE 802.15.4 standard.

After receiving 8 first symbols following the SFD, The MG2471 provide a correlation average value as a LQI. This is indicated by the LQI_VALID register. The value can be obtained by means of register read.

**LQICNF0 (LQI CONTROL0 REGISTER, 0x227E)**
This register is used to check LQI valid indicator.

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| [7] | LQI_VALID | LQI valid indicator : | RO | 0 |
| [6:4] | Reserved | Only ‘0’ allowed. | R/W | 0x0 |
| [3] | LQI_EN | LQI Enable Register<br>1 : Enable<br>0 : Disable | R/W | 0 |
| [2:0] | Reserved | Only ‘0’ allowed. | R/W | 0x0 |

**LQICNF1 (LQI CONTROL1 REGISTER,0x227F)**
This register is LQI value which is computed with correlation value.

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| [7:0] | LQI | LQI value : 0~ 255 | RO | 0x00 |

### 9.2.7. Received Signal Strength Indicator

When a packet is received, the baseband PHY provides both of the received signal strength Indicator (RSSI). The average energy level of the received RF signal at antenna is stored at AGCSTS2. The average energy level of the received packet is stored at AGCSTS3.

[Figure 23] shows typical measured RSSI plot over whole dynamic range. The typical dynamic range of the RSSI is about 80dB, and the accuracy is less than ± 3dB.

**AGCSTS2 (AGC STATUS2 REGISTER, 0x2284)**
The stored energy level is the average of the received signal energy. The indicated value at AGCSTS2 register is stored as a 2’s complement integer in dBm.

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| [7:0] | RXENRG | Average energy level of the received RF signal at antenna. | RO | 0x00 |

**AGCSTS3 (AGC STATUS3 REGISTER, 0x2285)**
While AGCSTS2 register indicates the average of received signal's energy level for a defined time interval, AGCSTS3 register shows the energy level of the last received packet. The value in AGCSTS3 register is retained until another packet is received.

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| [7:0] | PKTENRG | Average energy level of the received packet | RO | 0x00 |

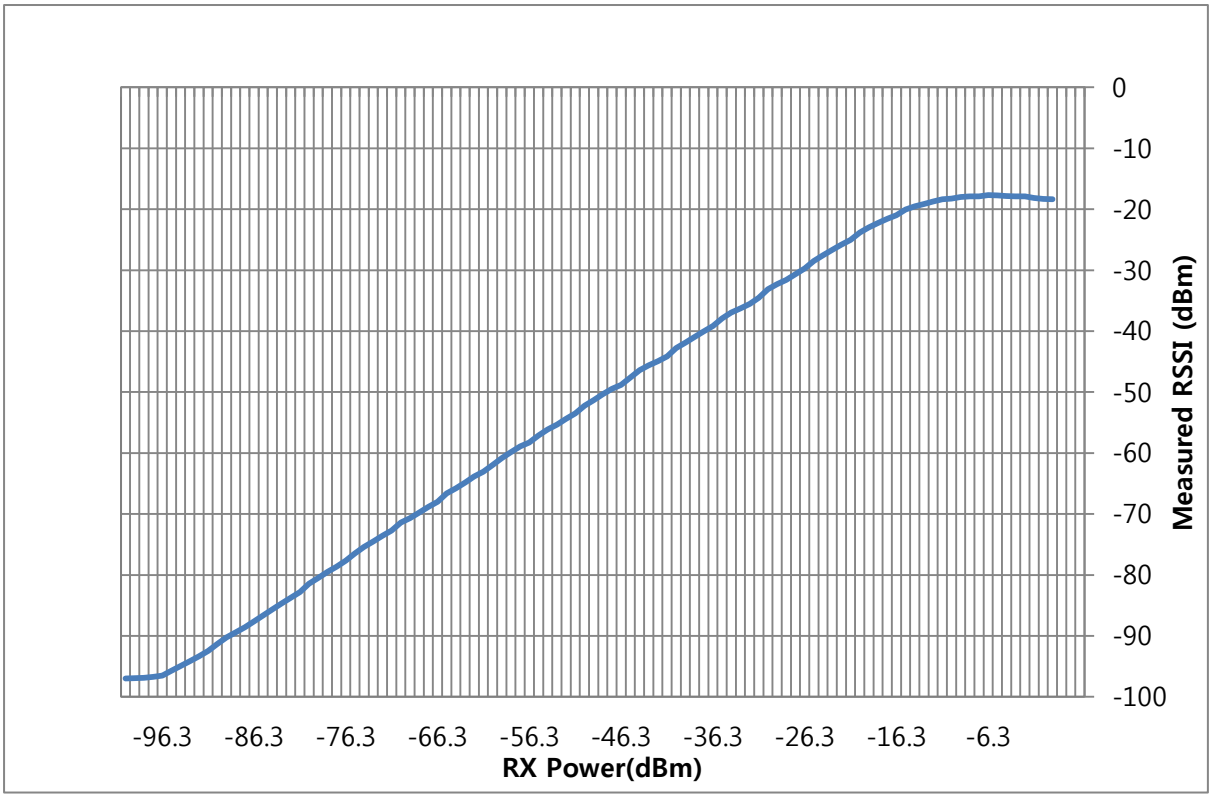



**Figure 24. Measured RSSI (typical) versus RX input power**

## 9.2.8. RADIO

A simplified block diagram with emphasis on RF and Analog front-end is shown in [Figure 25]. Since the bidirectional differential RF pins are used for RX and TX, no external T/R switch is required. In a receive path, a direct-conversion architecture is adopted. It operates in the 2.4GHz ISM band with excellent receiver sensitivity and robustness to interferers. Transmitter architecture is based on a direct-modulation technique using a direct RF frequency synthesis.

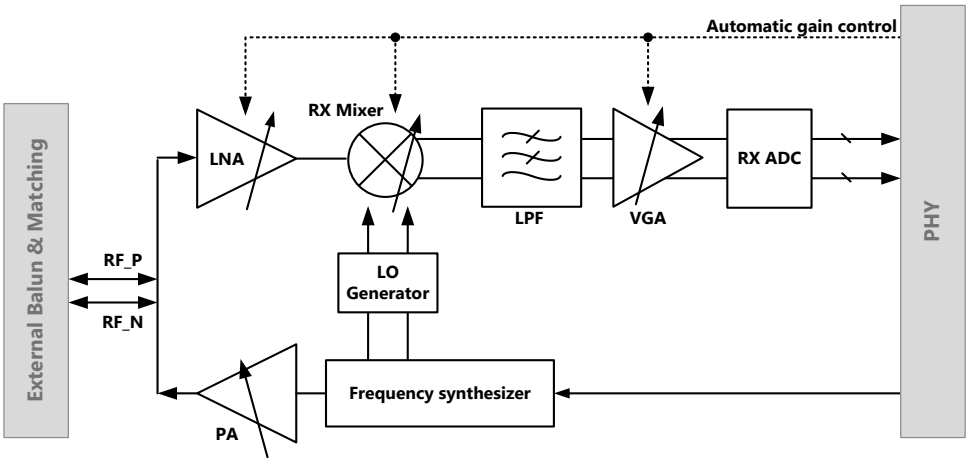



**Figure 25. RF and Analog Block Diagram**

The LNA amplifies the incoming received RF signal at RF_P and RF_N pins. The gain is controlled coarsely by the AGC block.

The RX Mixer converts the RF signal to the baseband frequency in quadrature(I and Q). Also, the gain is controlled coarsely by the AGC block.

Channel filtering occurs in the LPF(low-pass filter). The VGA(variable-gain amplifier) provides sufficient gain, controlled by AGC, to drive the RX ADC(analog-to-digital converter).

The RX ADC converts the VGA output signals to the signed binary digital signals.

The frequency synthesizer(PLL) generates the carrier signals for channel frequency during reception and feeds the baseband modulation signals directly to the power amplifier during transmission. The center frequency of the desired channel can be adjusted by PLLFREQ register.

The LO generator transforms the differential outputs of the frequency synthesizer into the quadrature(I and Q) signals required for local signals in the RX Mixer.

The TX PA(power amplifier) amplifies the modulated RF signal from the PLL. The transmit power can be controlled by setting two registers of TXPA and TXDA.

In addition, external PA can be used with control pin(s) of TRSW and/or TRSWB. The TRSW and TRSWB is shared with GPIO P1[7] and P1[6] respectively. When MG2471 stays at the transmit mode, TRSW = 1. These pins are available by setting two registers of P1SRC_SEL (SFR) and MONCON1.

**PLLFREQ (CHANNEL CENTER FREQUENCY CONTROL REGISTER, 0x22BF)**
This register is used to control the frequency of the frequency synthesizer for selecting the desired channel.

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| [7] | (Reserved) | Only '0' allowed. | R/W | 0 |
| [6:0] | PLL_FREQ | Channel center frequency selection register<br>$f_{center}$ = 2394 + PLL_FREQ (MHz)<br>The values of 5xN + 1 where N = 0, 1, ..., 22 are only valid as that of PLL_FREQ. | R/W | 0x33 |

**TXPA (TX PA CONTROL REGISTER, 0x22CE)**
This register is used to control the gain of the transmit PA along with TXDA.

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| [7:4] | (Reserved) | Only '0' allowed. | R/W | 0x0 |
| [3:0] | PA_GC | TX power amp control register<br>As the register control value increases form 0x0 to 0xF, the power increases. | R/W | 0xF |

**TXDA (TX DA CONTROL REGISTER, 0x22CF)**
This register is used to control the gain of the transmit PA along with TXPA.

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| [7:5] | (Reserved) | Only '0' allowed. | R/W | 0x0 |
| [4:0] | DA_GC | TX power amp control register<br>As the register control value increases form 0x0 to 0xF, the power increases. | R/W | 0x1F |

**P1SRC_SEL (GPIO 1 SOURCE CONTRL REGISTER, 0x9C (SFR))**
This register is used to control the GPIO source

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| [7:0] | P1SRC_SEL | PORT-1 source control register. Each bit of port-1 can be mapped to the specific signal correspondingly. With this register control of P1SRC_SEL = 0xC0, the TRSW and TRSWB which are drived by baseband modem are available through P1[7] and P1[6] respectively. | R/W | 0x00 |

**MONCON1 (MONITOR CONTROL REGISTER1, 0x2291)**
This register is used to generate the TRSW and TRSWB along with P1SRC_SEL.

| Bit Field | Name | Descriptions | RW | Reset Value |
|---|---|---|---|---|
| [7:0] | MONCON1 | Currently, only 0x00 is allowd.This setting of 0x00 generates the TRSW and TRSWB through P1[7] and P1[6]. | R/W | 0x00 |

## 9.3. Operating Modes

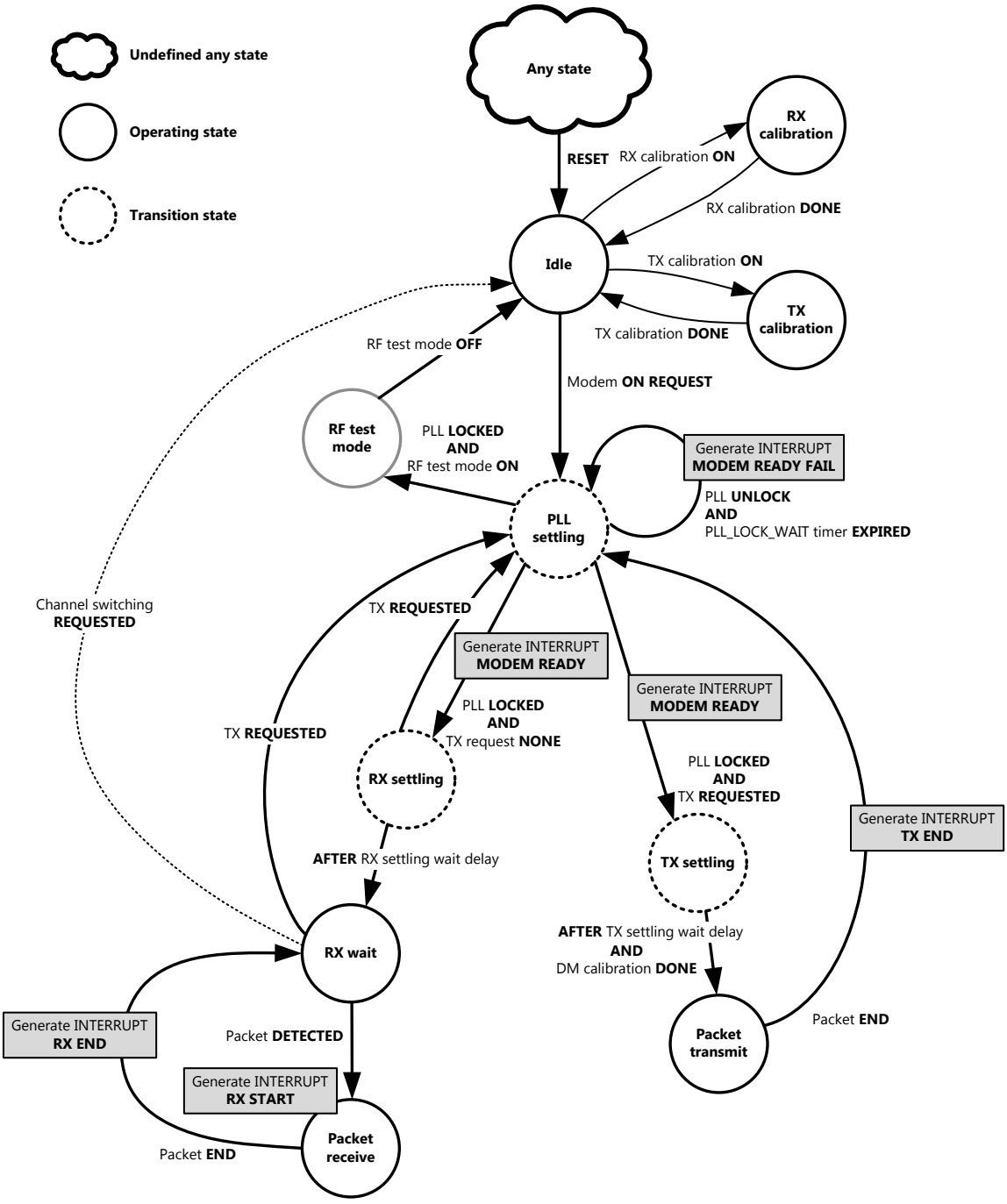



**Figure 26 MG2471 State transition diagram**

MG2471 PHY operation is controlled by the modem FSM shown in [Figure 26]. MG2471 PHY can be initialized by the reset. According to the control of the modem FSM, MG2471 operates in either packet transmitting or packet receiving mode. When the packet to be transmitted is prepared in TX MAC FIFO, MG2471 only operates in the packet transmit mode. Besides, it operates in the packet receiving mode and waits for the packet.

**Idle state**: MG2471 PHY can be initialized by the reset and the state of the modem FSM is moved to the idle state. In this state, the PHY executes no operation.

**RX calibration** state: In order to receive the packet correctly, the DC offset of the RF receiver should be calibrated before using it. Before MODEM ON is set, the DC offset of the RF receiver is preferred to be calibrated. When the DC calibration is initiated, the state is transited to RX calibration state. When the RX calibration has completed, the state is automatically transited to idle state. After the initial DC calibration is performed, the DC calibration tracker should be enabled.

**TX calibration** state: The modulation block of the RF transmitter should be also calibrated. Before MODEM ON is set, the TX modulator is preferred to be calibrated. When the TX calibration is initiated, the state is transited to TX calibration state. When the TX calibration has completed, the state is automatically transited to idle state.

**PLL settling** state: When the TX calibration is done, the RF synthesizer for channel selection can be configured and then the PLL (RF synthesizer) is started. Additionally, the PLL may be restarted in order to change the RX or TX channel. In the PLL settling state, the modem waits for the PLL to be locked. If the PLL is locked within designed time interval, the interrupt for MODEM READY is generated. Otherwise, the interrupt for MODEM READY FAIL is generated. This state is also a transition state. If the PLL is already locked (it can be clearly identified from the PLL lock detection flag), this state can be skipped.

**RF test mode** state: The RF test mode state is entered by setting the register as the RF test mode. When the PLL is locked and the RF test mode is set, the modem FSM changes its state from the PLL settling to the RF test mode state. Basically, in this state, the modem operates as the transmitter only. The modem FSM leaves this state to the idle state when the RF test mode becomes disabled.

**TX settling** state: When the PLL is locked and the packet transmission is requested (from MAC layer), the state of the modem FSM is changed from the PLL settling to the TX settling. In this state, the modem waits for the RF transmitter to be stable. The modem FSM stays at this state during the TX (settling) wait delay which can be configured.

**Packet transmit** state: After TX (settling) wait delay, the state of the modem FSM is transited to the packet transmit state. In this state, the modem transmits the packet in accordance to the PHY specification. When the packet transmission is completed, the state is moved to the PLL settling state along with generating the interrupt for TX END.

**RX settling** state: When the PLL is locked and no packet transmission is requested, the state of the modem FSM is changed from the PLL settling to the RX settling state in order to wait for packet coming from other transmitting units. In this state, the modem waits for the RF receiver to be stable. The modem FSM stays at this state during the RX (settling) wait delay which can be configured. If the packet transmission is requested when the state of the modem FSM stays at this state, the modem FSM changes its state from the RX settling to the PLL settling state.

**RX wait** state: After RX (settling) wait delay, the state of the modem FSM is transited to the RX wait state. In this state, the modem waits for the packet reception. When the packet is detected, the state is moved to the packet receive state along with generating the interrupt for RX START. If the packet transmission is requested when the state of the modem FSM stays at this state, the modem FSM changes its state from the RX wait to the PLL settling state.

**Packet receive** state: When the packet is detected at the RX wait state, the state of the modem FSM is moved to the packet receive state. In this state, the modem receives the packet and puts its payload to RX MAC FIFO. At the end of the packet, the state is transited to the RX wait state along with generating the interrupt for RX END.

# 10. IN-SYSTEM PROGRAMMING (ISP)

The in-system programming (ISP) function enables a user to download an application program to the internal flash memory. When it is power-on, the MG2471 checks the value of MS[2:0] pin. When the value of the MS[2] pin is ‘1’ and the value of the MS[1:0] is ‘0’, ISP mode is selected. The following procedure is to use the ISP function.

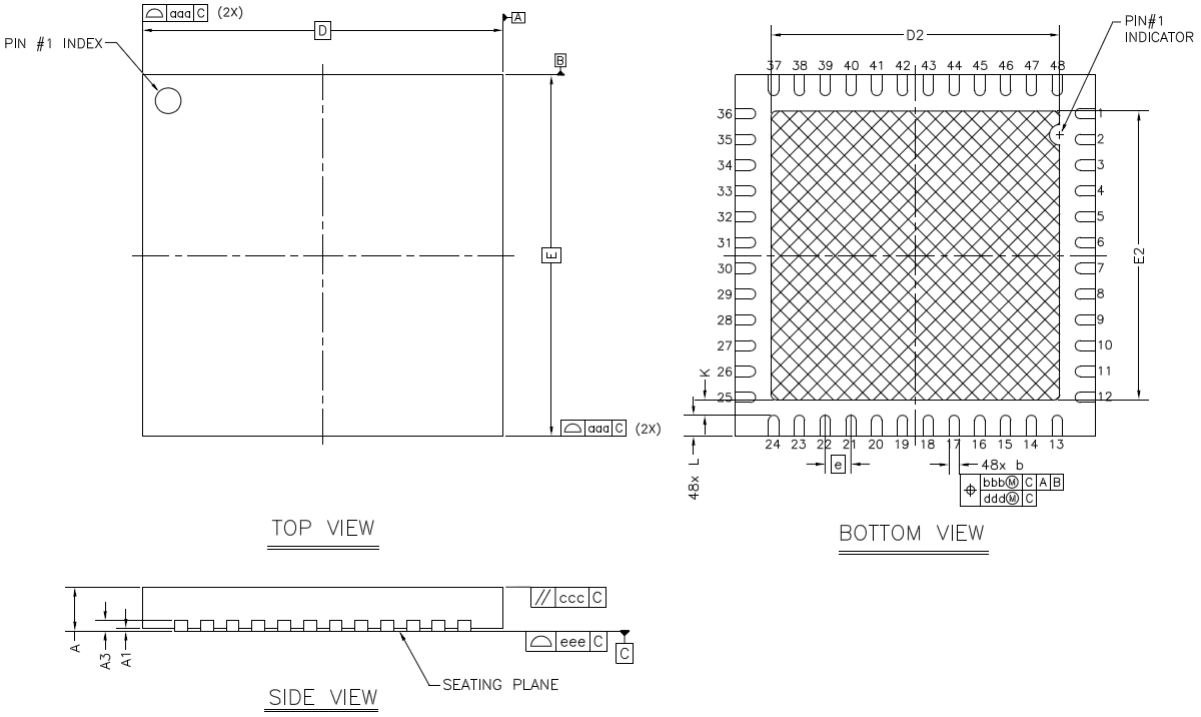
1. In MS[2:0] pin, MS[2] should be set to‘1’. MS[1] and MS[0] should be set to ‘0’.
2. Make RS-232 connection with the PC by using the serial port or the USB-to-Serial adapter. The configuration is 8-bit, no parity, 1 stop bit and 115200 baud rate.
3. Power up the device.
4. Execute the ISP Host program on PC. (It is included in Development Kit)
5. Load an application program in Intel HEX format.
6. Download.

When the procedure is finished, an application program is stored in the internal flash memory. To execute the application program, a device should be reset after setting MS[2:0] pin to ‘0’.

After reset, the application program in the internal flash memory is executed by the internal MCU.

# 11. PACKAGE INFORMATION

## 11.1. MG2471 Dimensions (QFN 48-pin)



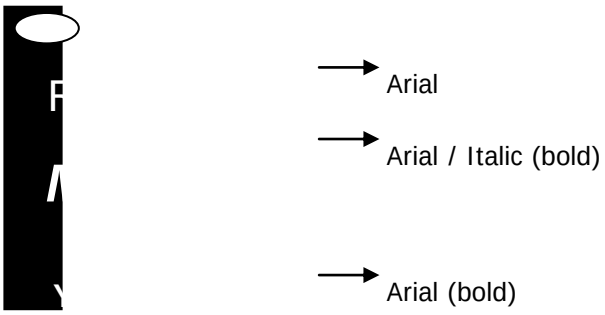

| COMMON DIMENSIONS | | | |
|---|---|---|---|
| SYMBOL | MIN. | NOM. | MAX. |
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF | |
| b | 0.15 | 0.20 | 0.25 |
| D | | 7.00 BSC | |
| E | | 7.00 BSC | |
| D2 | 5.45 | 5.60 | 5.75 |
| E2 | 5.45 | 5.60 | 5.75 |
| e | | 0.50 BSC | |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.15 | | |
| aaa | | 0.15 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |

NOTES :

1. DRAWING CONFORM TO JEDEC REFERENCE MO-220.
2. DIMENSIONING AND TOLERANCING SCHEMES CONFORM TO ASEM Y14.5M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. HATCH AREA IS SOLDERABLE EXPOSED PAD.

**Figure 27. Package Drawing-QFN48**

## 11.2. Marking




YY : represents the year of assembly
WW : two numbers representing the week of assembly
AA : capital letters which represent the order of the lots of any particular product being assembled in any one week. (01,02,...99)
C : Assembly house
X : Mask Version

**Figure 28. Chip Marking**

**RadioPulse Inc**

3rd Fl., Hans B/D II, 111-6 Seongnae-Dong,
Gangdong-Gu, Seoul, Korea, 134-883, Korea

URL: www.radiopulse.co.kr
Tel: +82-2-478-2963~5
Fax: +82-2-478-2967

sales@radiopulse.co.kr

## About RadioPulse Inc.

**RadioPulse** is a Being Wireless solution provider offering wireless communication & network technologies and developing next generation wireless networking technologies.

The new wireless networking solutions envisioned by RadioPulse will enable user to enjoy wireless technologies with easy interface.

Founded in April of 2003, the company maintains it headquarters and R&D center in Seoul, Korea.