

## Evaluating the **ADN8835** Ultracompact, 3 A Thermoelectric Cooler (TEC) Controller

### FEATURES

Full featured evaluation board for the **ADN8835**; the device includes the following features:

- Complete TEC controller with integrated 3 A TEC driver
- Operating voltage range:  $V_{IN} = 2.7\text{ V to }5.5\text{ V}$
- TEC voltage and current operation monitoring
- Independent TEC heating and cooling current-limit settings
- Programmable maximum TEC voltage
- External synchronization from 1.85 MHz to 3.25 MHz
- 2.5 V reference output
- Input for NTC thermistor connection
- Output for TEC module wires
- Disable jumper
- 45 mm × 25 mm evaluation board size

### GENERAL DESCRIPTION

The **ADN8835CP-EVALZ** is a configurable evaluation board designed to work with various TEC modules and thermistors. The **ADN8835**, which is included on the evaluation board, delivers and controls bidirectional current through a TEC controller using two pairs of the complementary integrated MOSFETs in an H bridge configuration.

The TEC cooling and heating current limits are set to 3 A, and the maximum TEC voltage is programmed to 3.5 V using two on-board resistor dividers. The temperature setpoint circuit is optimized to work with a 10 k $\Omega$  negative thermal coefficient (NTC) thermistor. The on-board proportional integral differential (PID) compensation network components can be replaced by soldering different value components that match the temperature

### ADN8835CP-EVALZ EVALUATION BOARD

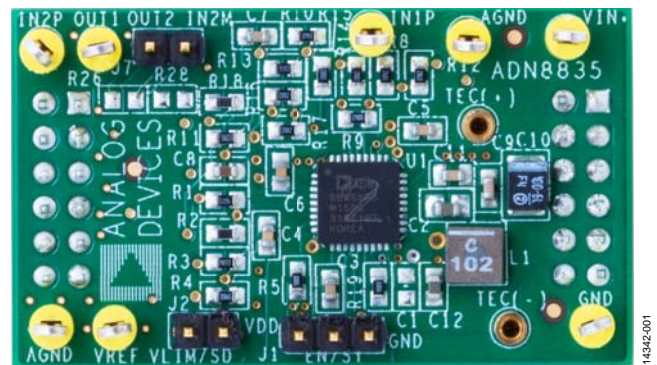


Figure 1.

control loop characteristics with the thermal load to achieve the required response time and temperature stability. The cooling and heating TEC current limits and maximum TEC voltage setting can also be modified by changing the values of the corresponding components.

In addition, the board can be plugged into the **ADN8835** base board, which has adjustable components for the tunable analog thermal PID network, the temperature setpoint, and the maximum TEC current and TEC voltage limits.

Full specifications on the **ADN8835** are available in the **ADN8835** data sheet, which should be consulted in conjunction with this user guide when working with the evaluation board.

**TABLE OF CONTENTS**

Features .....	1	Reading the TEC Voltage .....	5
ADN8835CP-EVALZ Evaluation Board.....	1	Reading the TEC Current .....	5
General Description .....	1	TEC Driver Control .....	5
Revision History .....	2	Using ADN8835 the Base Board .....	6
Using the Evaluation Board.....	3	Evaluation Board Schematics and Artwork.....	7
Board Connection .....	3	Ordering Information.....	12
Maximum TEC Cooling Voltage.....	3	Bill of Materials.....	12
Cooling and Heating TEC Current Limits.....	4		
PWM Operation Frequency .....	4		

**REVISION HISTORY**

12/2016—Revision 0: Initial Version

# USING THE EVALUATION BOARD

## BOARD CONNECTION

Apply a power source to the VIN+ and GND terminals. Connect the TEC module to the TEC(+) and TEC(-) terminals. Connect the thermistor to the THERM and AGND terminals. The power source voltage must be between 2.7 V and 5.5 V, which matches the power supply range of the ADN8835. Connect the EN/SY pin to VDD (on the board) and remove the shunt from the VLIM/SD jumper to enable the controller.

## MAXIMUM TEC COOLING VOLTAGE

The maximum TEC cooling voltage is set to 3.5 V by the values of  $R_{V1} = 4.29 \text{ k}\Omega$  and  $R_{V2} = 10 \text{ k}\Omega$ .

To change this setting, modify the value of  $R_{V1}$  using the equations provided in the Using a Resistor Divider to Set the TEC Voltage Limit section (for more information, refer to the ADN8835 data sheet) or by following the recommended values in Table 1.

## Using a Resistor Divider to Set the TEC Voltage Limit

Calculate the cooling and heating limits using the following equations:

$$V_{VLIMC} = V_{REF} \times R_{V2} / (R_{V1} + R_{V2}) \tag{1}$$

where  $V_{REF} = 2.5 \text{ V}$ .

$$V_{VLIMH} = V_{VLIM\_COOLING} - I_{SINK\_VLIM} \times R_{V1} \parallel R_{V2} \tag{2}$$

where  $I_{SINK\_VLIM} = 10 \mu\text{A}$  (see Figure 2).

$$V_{TEC\_MAX\_COOLING} = V_{VLIM\_COOLING} \times A_{VLIM} \tag{3}$$

where  $A_{VLIM} = 2 \text{ V/V}$ .

$$V_{TEC\_MAX\_HEATING} = V_{VLIM\_HEATING} \times A_{VLIM} \tag{4}$$

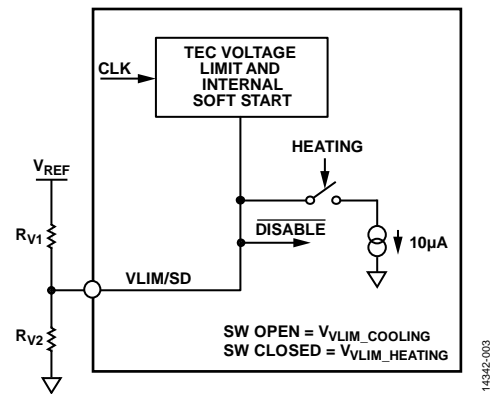


Figure 2. Programming the Maximum TEC Voltage

Table 1. Setting the Maximum TEC Voltage ( $R_{V2} = 10 \text{ k}\Omega$ )

$V_{TEC\_MAX\_COOLING} \text{ (V)}^1$	$V_{VLIMC} \text{ (V)}^2$	$R_{V1} \text{ (k}\Omega)^3$	$V_{TEC\_COOLING} \text{ (V)}^4$	$R_{V1} \parallel R_{V2} \text{ (k}\Omega)^3$	$V_{VLIMH} \text{ (V)}^5$	$V_{TEC\_MAX\_HEATING} \text{ (V)}^6$	$V_{TEC\_HEATING} \text{ (V)}^7$
4.750	2.375	0.53	2.438	0.5	2.370	4.740	0.065
4.500	2.250	1.11	2.375	1.0	2.240	4.480	0.130
4.250	2.125	1.76	2.313	1.5	2.110	4.220	0.195
4.000	2.000	2.50	2.250	2.0	1.980	3.960	0.260
3.750	1.875	3.33	2.188	2.5	1.850	3.700	0.325
3.500	1.750	4.29	2.125	3.0	1.720	3.440	0.390
3.250	1.625	5.38	2.063	3.5	1.590	3.180	0.455
3.000	1.500	6.67	2.000	4.0	1.460	2.920	0.520
2.750	1.375	8.18	1.938	4.5	1.330	2.660	0.585
2.500	1.250	10.00	1.875	5.0	1.200	2.400	0.650
2.250	1.125	12.22	1.813	5.5	1.070	2.140	0.715
2.000	1.000	15.00	1.750	6.0	0.940	1.880	0.780
1.750	0.875	18.57	1.688	6.5	0.810	1.620	0.845
1.500	0.750	23.33	1.625	7.0	0.680	1.360	0.910
1.250	0.625	30.00	1.563	7.5	0.550	1.100	0.975
1.000	0.500	40.00	1.500	8.0	0.420	0.840	1.040
0.750	0.375	56.67	1.438	8.5	0.290	0.580	1.105
0.500	0.250	90.00	1.375	9.0	0.160	0.320	1.170
0.250	0.125	190.00	1.313	9.5	0.030	0.060	1.235

<sup>1</sup>  $V_{TEC\_MAX\_COOLING}$  is the maximum target TEC voltage when the ADN8835 operates in cooling mode.  
<sup>2</sup>  $V_{VLIMC}$  is the voltage set at the VLIM/SD input pin for cooling.  
<sup>3</sup>  $R_{V1}$  is the required value of Resistor R1.  $R_{V2}$  is the required value of Resistor R2.  
<sup>4</sup>  $V_{TEC\_COOLING}$  is the voltage at the VTEC output when the TEC voltage reaches the maximum limit in cooling mode.  
<sup>5</sup>  $V_{VLIMH}$  is the voltage set at the VLIM/SD input pin for heating.  
<sup>6</sup>  $V_{TEC\_MAX\_HEATING}$  is the maximum TEC voltage set when the ADN8835 operates in heating mode.  
<sup>7</sup>  $V_{TEC\_HEATING}$  is the voltage at the VTEC output when the TEC voltage reaches the maximum limit in heating mode.

**COOLING AND HEATING TEC CURRENT LIMITS**

The maximum TEC cooling and heating current limits are both set to 1.5 A by the values of the resistors,  $R_{C3} = 270.6 \text{ k}\Omega$  and  $R_{C4} = 50.8 \text{ k}\Omega$ . To change these settings, use the equations provided in the Using a Resistor Divider to Set the TEC Current Limit section (for more information, refer to the ADN8835 data sheet) or use the values recommended in Table 3.

**Using a Resistor Divider to Set the TEC Current Limit**

Use the following equations to calculate the maximum TEC currents:

$$V_{ILIMH} = V_{REF} \times R_{C2} / (R_{C1} + R_{C2}) \tag{5}$$

where  $V_{REF} = 2.5 \text{ V}$ .

$$V_{ILIMC} = V_{ILIMH} + I_{SINK\_ILIM} \times R_{C1} \parallel R_{C2} \tag{6}$$

where  $I_{SINK\_ILIM} = 40 \text{ }\mu\text{A}$ .

$$I_{TEC\_MAX\_COOLING} = \frac{V_{ILIM\_COOLING} - 1.25 \text{ V}}{R_{CS}} \tag{7}$$

where  $R_{CS} = 0.285 \text{ V/A}$ .

$$I_{TEC\_MAX\_HEATING} = \frac{1.25 \text{ V} - V_{ILIM\_HEATING}}{R_{CS}} \tag{8}$$

$V_{ILIMH}$  must not exceed 1.2 V and  $V_{ILIMC}$  must be more than 1.3 V to leave proper margins between the heating and the cooling modes.

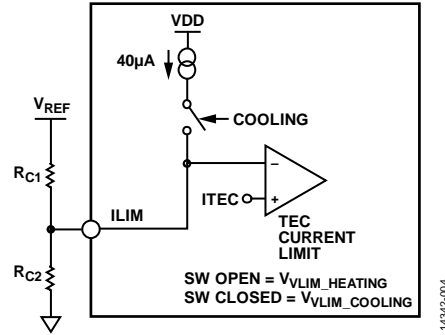


Figure 3. Programming the TEC Current Cooling and Heating Limits

**PWM OPERATION FREQUENCY**

The frequency of the pulse-width modulation (PWM) TEC driver stage can be configured at the 3-pin jumper, J1. Apply the external synchronization clock signal to the middle pin of the jumper. Note that the middle pin can also be used to shut down the device when it is pulled below 0.8 V. Therefore, when applying the external clock signal, ensure that the high level is greater than 2.1 V and the low level is less than 0.8 V. The combinations of the EN/SY pin settings are shown in Table 2.

Table 2. EN/SY Pin Settings

EN/SY Pin State	PWM Operation Frequency
Low (<0.8 V)	Shutdown
Open	Shutdown
High (>2.1 V)	2 MHz
External clock signal (high > 2.1 V, low < 0.8 V)	From 1.85 MHz to 3.25 MHz

Table 3. Values of the Resistor Divider for ILIM Settings

$I_{TEC\_MAX\_COOLING} \text{ (A)}^1$	$V_{ILIMC} \text{ (V)}^2$	$I_{TEC\_MAX\_HEATING} \text{ (A)}^3$	$V_{ILIMH} \text{ (V)}^4$	$R_{C1} \text{ (k}\Omega)^5$	$R_{C2} \text{ (k}\Omega)^5$	$R_{C1} \parallel R_{C2} \text{ (k}\Omega)^5$
3.0	2.105	-3.0	0.395	270.6	50.8	42.750
2.9	2.077	-2.9	0.424	243.9	49.8	41.325
2.8	2.048	-2.8	0.452	220.7	48.7	39.900
2.7	2.020	-2.7	0.481	200.2	47.6	38.475
2.6	1.991	-2.6	0.509	182.0	46.5	37.050
2.5	1.963	-2.5	0.538	165.7	45.4	35.625
2.4	1.934	-2.4	0.566	151.1	44.2	34.200
2.3	1.906	-2.3	0.595	137.8	43.0	32.775
2.2	1.877	-2.2	0.623	125.8	41.8	31.350
2.1	1.849	-2.1	0.652	114.8	40.5	29.925
2.0	1.820	-2.0	0.680	104.8	39.1	28.500

$I_{TEC\_MAX\_COOLING}$ (A) <sup>1</sup>	$V_{ILIMC}$ (V) <sup>2</sup>	$I_{TEC\_MAX\_HEATING}$ (A) <sup>3</sup>	$V_{ILIMH}$ (V) <sup>4</sup>	$R_{C1}$ (k $\Omega$ ) <sup>5</sup>	$R_{C2}$ (k $\Omega$ ) <sup>5</sup>	$R_{C1}  R_{C2}$ (k $\Omega$ ) <sup>5</sup>
1.9	1.792	-1.9	0.709	95.5	37.8	27.075
1.8	1.763	-1.8	0.737	87.0	36.4	25.650
1.7	1.735	-1.7	0.766	79.1	34.9	24.225
1.6	1.706	-1.6	0.794	71.8	33.4	22.800
1.5	1.678	-1.5	0.823	65.0	31.9	21.375
1.4	1.649	-1.4	0.851	58.6	30.2	19.950
1.3	1.621	-1.3	0.880	52.7	28.6	18.525
1.2	1.592	-1.2	0.908	47.1	26.9	17.100
1.1	1.564	-1.1	0.937	41.8	25.1	15.675
1.0	1.535	-1.0	0.965	36.9	23.2	14.250

<sup>1</sup>  $I_{TEC\_MAX\_COOLING}$  is the maximum target TEC current when the ADN8835 operates in cooling mode.

<sup>2</sup>  $V_{ILIMC}$  is the voltage set at the ILIM pin when the ADN8835 operates in cooling mode.

<sup>3</sup>  $I_{TEC\_MAX\_HEATING}$  is the maximum target TEC current when the ADN8835 operates in heating mode.

<sup>4</sup>  $V_{ILIMH}$  is the voltage set at the ILIM pin when the ADN8835 operates in heating mode.

<sup>5</sup>  $R_{C1}$  is the required value of Resistor R3.  $R_{C2}$  is the required value of Resistor R4.

## READING THE TEC VOLTAGE

The voltage on the VTEC output pin is proportional to the voltage across the TEC and is measured at Connector J6/Pin 11. The relationship between the voltage on the VTEC output and the voltage across the TEC is as follows:

$$V_{TEC} = V_{LDR} - V_{SFB} = 4 \times (V_{VTEC} - 0.5 \times V_{REF}) \quad (9)$$

where:

$V_{TEC}$  is the voltage across the TEC.

$V_{LDR}$  is the voltage measured at the LDR pin.

$V_{SFB}$  is the voltage measured at the SFB pin.

$V_{VTEC}$  is the voltage measured at the VTEC pin.

$V_{REF}$  is the reference voltage, 2.5 V.

## READING THE TEC CURRENT

The voltage on the ITEC output pin is proportional to the TEC current, and is measured at Connector J6/Pin 12. Calculate the TEC current ( $I_{TEC}$ ) from the ITEC pin voltage as follows:

$$I_{TEC} = \frac{V_{ITEC} - 0.5 \times V_{REF}}{R_{CS}} \quad (10)$$

where:

$I_{TEC}$  is the TEC current, defined as the current flowing into the positive TEC terminal (TEC+) and out of the negative TEC terminal (TEC-).

$V_{ITEC}$  is the voltage measured at the ITEC pin.

$V_{REF}$  is the reference voltage, 2.5 V.

$R_{CS}$  is the current sense gain, 0.285 V/A.

## TEC DRIVER CONTROL

The TEC driver has a linear driver (LDR) and a PWM driver with an SW output and a voltage feedback input pin (SFB). The TEC driver is controlled by the voltage signal at the OUT2 pin. The equations for the linear and PWM driver outputs, respectively, are as follows:

$$V_{LDR} = V_B - 40 (V_{OUT2} - 1.25 \text{ V}) \quad (11)$$

$$V_{SFB} = V_{LDR} + 5 (V_{OUT2} - 1.25 \text{ V}) \quad (12)$$

where:

$V_{LDR}$  is the voltage at the liner driver output.

$V_B$  is determined by voltage at the VDD pin ( $V_{VDD}$ ) as follows:

$$V_B = 1.5 \text{ V} (V_{VDD} < 4.0 \text{ V}) \quad (13)$$

$$V_B = 2.5 \text{ V} (V_{VDD} > 4.0 \text{ V}) \quad (14)$$

$V_{OUT2}$  is the voltage at the OUT2 pin.

$V_{SFB}$  is the voltage at the PWM driver output.

The  $V_{LDR}$  and  $V_{SFB}$  voltages are limited by the power supply voltage with the upper limit of  $V_{VDD}$  and the lower limit of 0 V.

The voltage at the OUT2 pin is determined by the compensation amplifier with the PID network. This amplifier receives the temperature setpoint voltage at the IN2P input pin and the thermistor voltage at the IN2N pin, fed by the OUT1 pin of the error amplifier.

If the digital temperature control loop is used, configure the compensation amplifier as a unity-gain follower by connecting the OUT2 pin to the IN2N pin, and then apply the control signal from a digital-to-analog converter (DAC) to the IN2P input. Thus, the OUT2 pin voltage is equal to the DAC voltage at the IN2P pin, and the TEC driver outputs follow Equation 11 and Equation 12.

## USING THE ADN8835 BASE BOARD

The [ADN8835](#) base board, which is compatible with the [ADN8833](#), [ADN8834](#), and [ADN8835](#), is available upon request. The base board allows the user to tune the PID components in an analog thermal control loop due to the set of selectable R and C values (these values are on the base board). In addition, the base board offers adjustable components that allow the user to change the maximum TEC voltage and cooling and heating current limits. The temperature setpoint can be also changed manually by connecting an [ADN8835CP-EVALZ](#) board to the base board as the daughter card. To avoid duplication, remove several configuration components from the daughter card before connecting it into the [ADN8835](#) base board (see Table 4). Align the silkscreen labels on the two boards in the same orientation when plugging in.

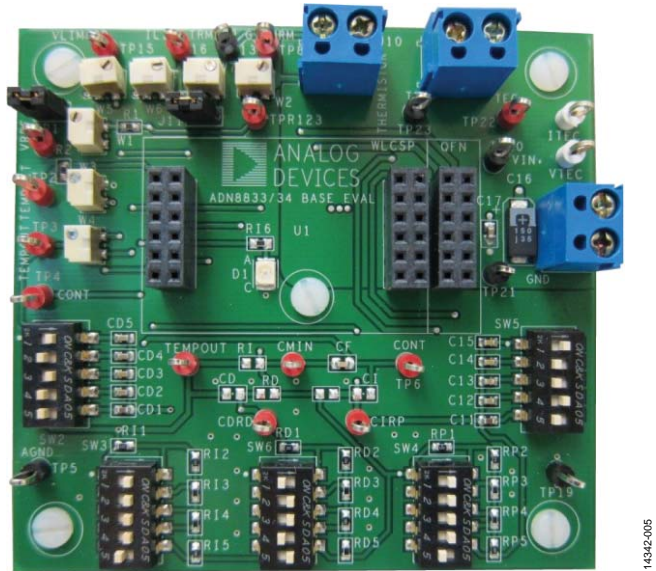


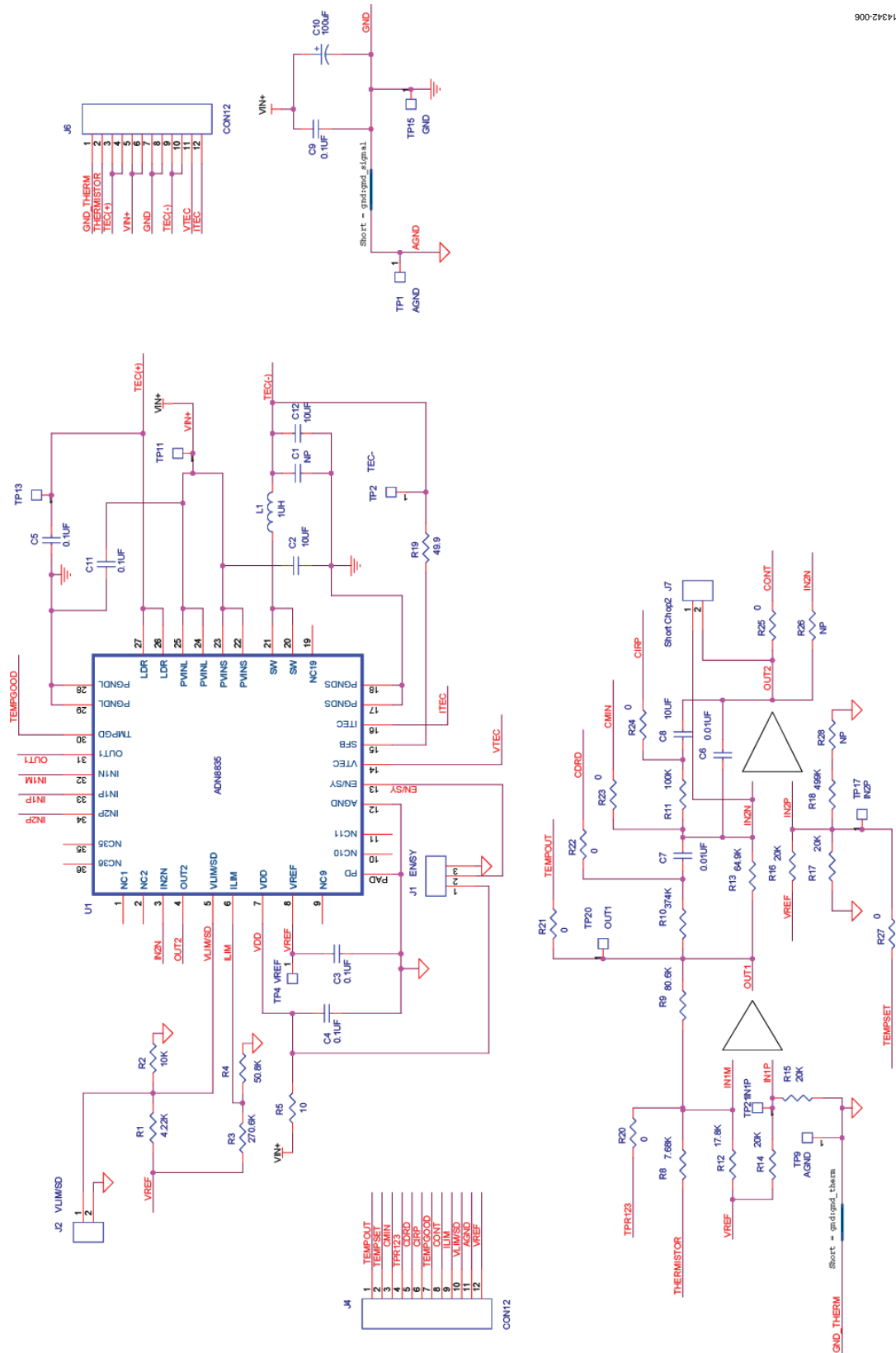
Figure 4. [ADN8835](#) Base Board (Compatible with the [ADN8833](#), [ADN8834](#), and [ADN8835](#))

Table 4. Configuration Components to Be Removed from the [ADN8835CP-EVALZ](#) Board

Component	Value	Function
R1	4.22 kΩ	Voltage limit (VLIM)
R3	270.6 kΩ	Current limit (ILIM)
R4	50.8 kΩ	ILIM
R10	165 kΩ	PID compensation amplifier
C7	10 μF	PID compensation amplifier
R13	1.87 MΩ	PID compensation amplifier
R16	20 kΩ	Temperature setpoint (TEMPSET)
R17	20 kΩ	TEMPSET
R11	1.87 MΩ	PID compensation amplifier
C8	1.5 μF	PID compensation amplifier
C6	0.01 μF	PID compensation amplifier
R9	80.6 kΩ	Thermistor amplifier
R8	7.68 kΩ	Thermistor amplifier
R12	17.8 kΩ	Thermistor amplifier

14342-005

# EVALUATION BOARD SCHEMATICS AND ARTWORK



14342-006

Figure 5. ADN8835CP-EVALZ Evaluation Board Schematic

14342-008

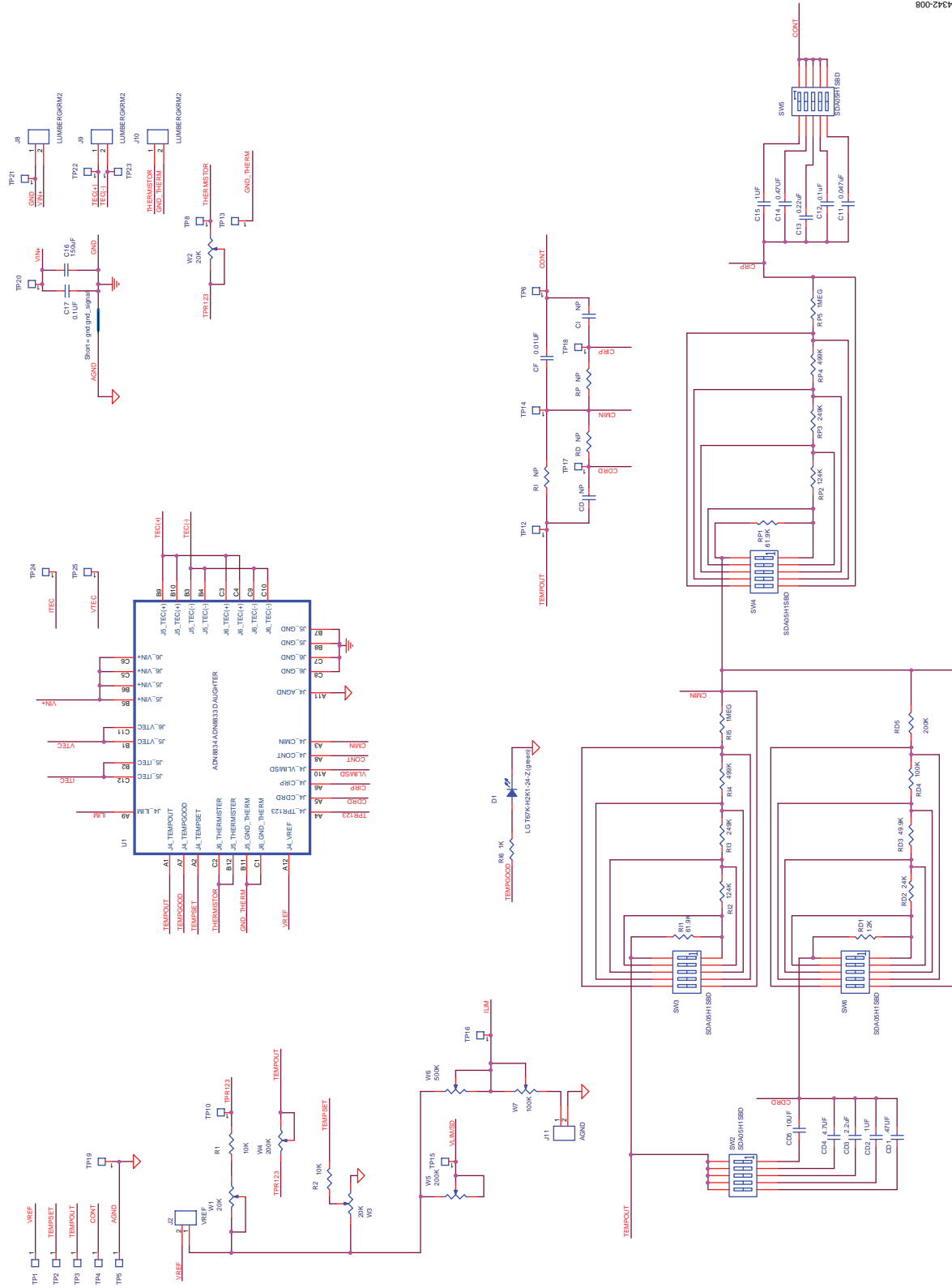


Figure 6. ADN8835 Base Board Schematic



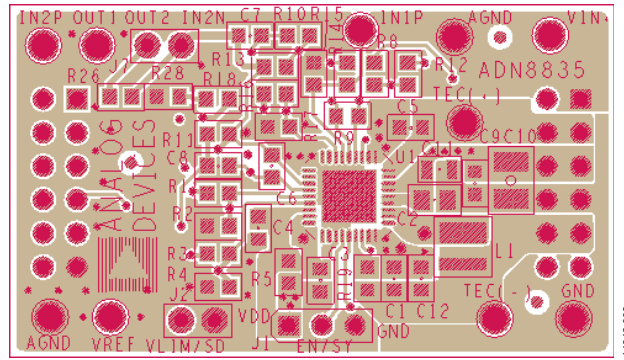


Figure 7. ADN8835CP-EVALZ Evaluation Board, Top Layer

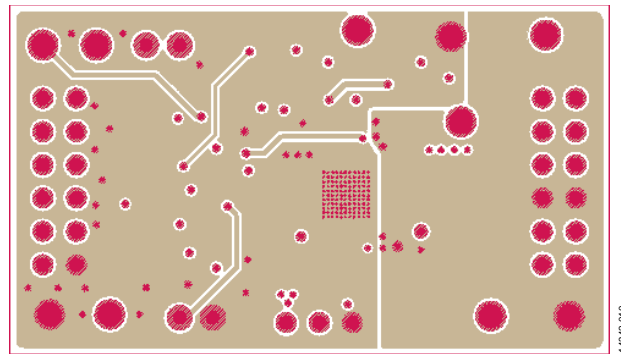


Figure 8. ADN8835CP-EVALZ Evaluation Board, Second Layer

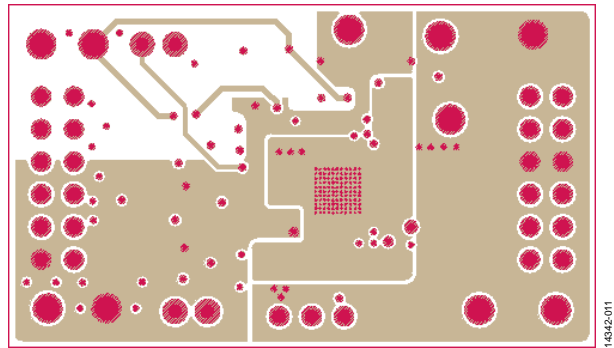


Figure 9. ADN8835CP-EVALZ Evaluation Board, Third Layer

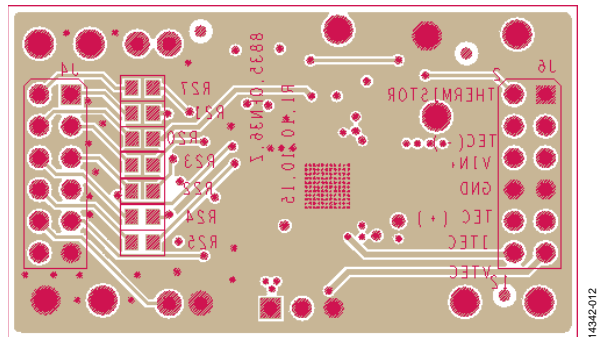


Figure 10. ADN8835CP-EVALZ Evaluation Board, Bottom Layer

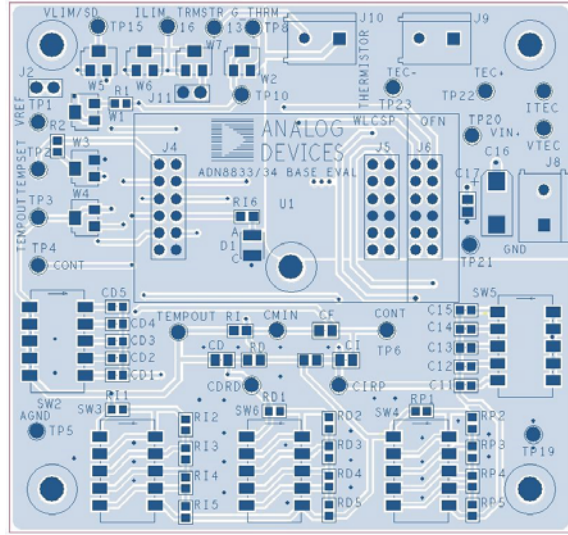


Figure 11. ADN8835 Base Board, Top Layer

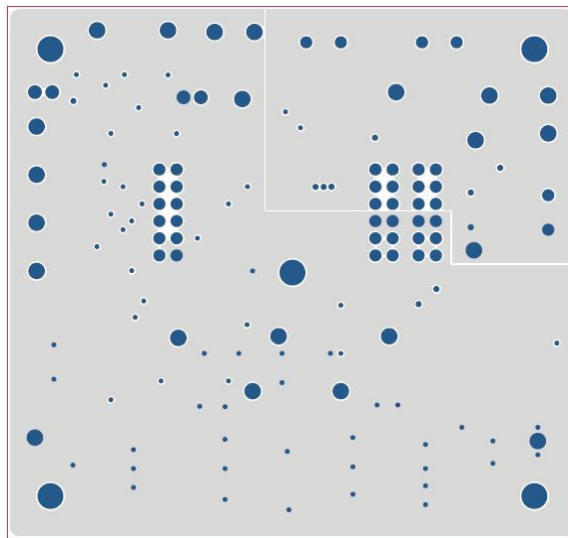


Figure 12. ADN8835 Base Board, Layer 2

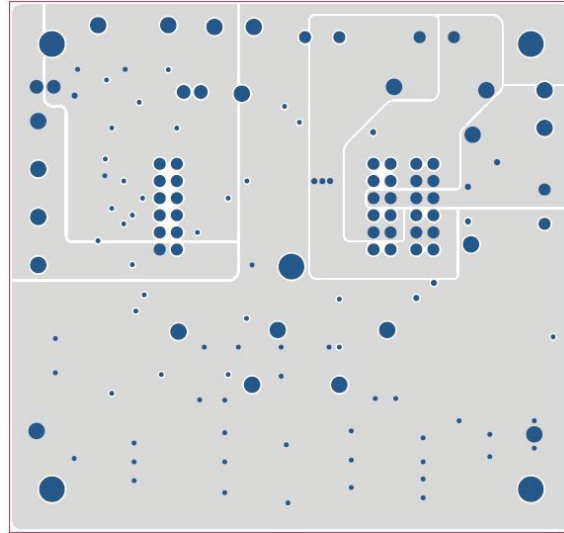


Figure 13. ADN8835 Base Board, Layer 3

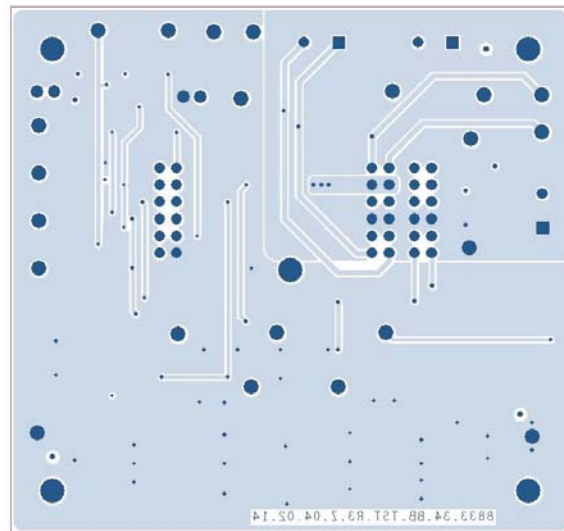


Figure 14. ADN8835 Base Board, Bottom Layer

## ORDERING INFORMATION

## BILL OF MATERIALS

Table 5. Bill of Materials for the [ADN8835CP-EVALZ](#) Evaluation Board

Quantity	Reference	Description	Manufacturer	Part Number
3	C2, C8, C12	Ceramic capacitor, 10 $\mu$ F, 10 V, 10%, X7R 0805	Taiyo Yuden	LMK212B7106KG-TD
5	C3, C4, C5, C9, C11	Ceramic capacitor, 0.1 $\mu$ F, 10 V, 10%, X7R 0603	Kemet	C0603C104K8RACTU
2	C6, C7	Ceramic capacitor, 0.01 $\mu$ F, 50 V, 10%, X7R 0603	Kemet	C0603C103K5RACTU
1	C10	Tantalum capacitor, 100 $\mu$ F, 6.3 V, 20%, 1411	Vishay	293D107X06R3B2T
1	J1	Jumper, 3-pin	Samtec	TSW-103-08-G-S
1	J2	Jumper, 2-pin	Samtec	TSW-103-08-G-S
2	J4, J6	Connector, double row, male, 12-pin	Samtec	TSW-112-08-G-D
1	L1	Inductor, 1 $\mu$ H	Coilcraft	XFL4020-102MEB
1	R1	Resistor, 4.22 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	CRCW06036K65FKEA
1	R2	Resistor, 10 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	ERJ-3EKF1002V
1	R3	Resistor, 274 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	CRCW0603210KFKEA
1	R4	Resistor, 51.1 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	CRCW060348K7FKEA
1	R5	Resistor, 10.0 $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	CRCW060310R0FKEA
1	R8	Resistor, 7.68 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	CRCW06037K68FKEA
1	R9	Resistor, 80.6 k $\Omega$ 1/10 W, 1%, 0603, SMD	Vishay	CRCW060380K6FKEA
1	R12	Resistor, 17.8 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	CRCW060317K8FKEA
1	R10	Resistor, 374 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	CRCW0603374KFKEA
1	R11	Resistor, 562 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	CRCW0603562KFKEA
1	R13	Resistor, 64.9 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	CRCW060364K9FKEA
4	R14, R15, R16, R17	Resistor, 20.0 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	CRCW060320K0FKEA
1	R18	Resistor, 499 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	ERJ-3EKF4993V
1	R19	Resistor, 49.9 $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	CRCW060349R9FKEA
7	R20, R21, R22, R23, R24, R25, R27	Resistor, 0.0 $\Omega$ , 1/10 W, 0603, SMD	Vishay	ERJ-3GEY0R00V
10	TP1, TP4, TP9, TP13, TP15, TP17, TP18, TP19, TP20, TP21	Test point	Keystone	5010
2	TP2, TP11	Connector	Mill-Max	3102-2-00-21-00-08-0
1	U1	Ultracompact, 3 A, TEC controller, LFCSP package	Analog Devices, Inc.	<a href="#">ADN8835ACPZ-R7</a>

Table 6. Bill of Materials for the [ADN8835](#) Base Board

Quantity	Reference	Description	Manufacturer	Part Number
2	CD1, C14	Ceramic capacitor, 0.47 $\mu$ F, 16 V, 10%, X5R, 0603	TDK	C1608X5R1C474K080AA
2	CD2, C15	Ceramic capacitor, 1 $\mu$ F, 16 V, 10%, X5R, 0603	Murata	GRM188R61C105KA
1	CD3	Ceramic capacitor, 2.2 $\mu$ F, 16 V, 10%, X5R, 0603	Murata	GRM188R61C225KE
1	CD4	Ceramic capacitor, 4.7 $\mu$ F, 6.3 V, 10%, X5R, 0603	Murata	GRM188R60J475KE19D
1	CD5	Ceramic capacitor, 10 $\mu$ F, 6.3 V, 20%, X5R, 0603	Panasonic	ECJ-1VB0J106M
1	CF	Ceramic capacitor, 0.01 $\mu$ F, 50 V, 10%, X7R, 0603	Kemet	C0603C103K5RACTU
1	C11	Ceramic capacitor, 0.047 $\mu$ F, 6.3 V, 10%, X5R, 0603	Murata	GRM033R60J473KE19D
2	C12, C17	Ceramic capacitor, 0.1 $\mu$ F, 50 V, 10%, X7R, 0603	AVX	06035C104KAT2A
1	C13	Ceramic capacitor, 0.22 $\mu$ F, 6.3 V, 10%, X5R, 0603	TDK	C0603X5R0J224K030BB
1	C16	Tantalum capacitor, 150 $\mu$ F, 6.3 V, 20%, 2917	Sanyo	6TPE150MI
1	D1	LED, green, 570 nm, clear, 2-PLCC	OSRAM	LG T67K-H2K1-24-Z
2	J2, J11	Jumper, 2-pin	Samtec	TSW-150-07-G-S
3	J8, J9, J10	Connector, PCB terminal, black, 2-pin	On Shore	OSTVN02A150

Quantity	Reference	Description	Manufacturer	Part Number
1	RD1	Resistor, 12 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	CRCW060312K0FKEA
1	RD2	Resistor, 24.3 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	CRCW060324K3FKEA
1	RD3	Resistor, 49.9 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Panasonic	ERJ-3EKF4992V
1	RD4	Resistor, 100 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	CRCW0603100KFKEA
1	RD5	Resistor, 200 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Panasonic	ERJ-3EKF2003V
2	RP1, RI1	Resistor, 61.9 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	CRCW060361K9FKEA
2	RP2, RI2	Resistor, 124 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	CRCW0603124KFKEA
2	RP3, RI3	Resistor, 249 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Panasonic	ERJ-3EKF2493V
2	RP4, RI4	Resistor, 499 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Panasonic	ERJ-3EKF4993V
2	RP5, RI5	Resistor, 1 M $\Omega$ , 1/10 W, 1%, 0603, SMD	Vishay	CRCW06031M00FKEA
1	RI6	Resistor, 1 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Panasonic	ERJ-6ENF4123V
2	R1, R2	Resistor, 10 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Panasonic	ERJ-3EKF1002V
5	SW2, SW3, SW4, SW5, SW6	Switch, low profile DIP, top slide, 5-position	C&K	SDA05H15BD
18	TP1, TP2, TP3, TP4, TP5, TP6, TP8, TP10, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21	Test point	Keystone	5010
1	U1	Connector <sup>1</sup>	Samtec	SSW-106-01-G-D
3	W1, W2, W3	Trimmer, 20 k $\Omega$ , 0.25 W, SMD	Murata	PVG5A203C03R00
2	W4, W5	Trimmer, 200 k $\Omega$ , 0.25 W, SMD	Murata	PVG5A204C03R00
1	W6	Trimmer, 500 k $\Omega$ , 0.25 W, SMD	Murata	PVG5A504C03R00
1	W7	Trimmer, 100 k $\Omega$ , 0.25 W, SMD	Murata	PVG5A104C03R01

<sup>1</sup> U1 has a reserved area to plug in the daughter board. The silkscreen mark includes three 12-pin female connectors and several other components.



#### ESD Caution

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

#### Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS (\$100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

©2016 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.  
UG14342-0-12/16(0)



www.analog.com