Memory Module Data Sheet

Product Model Name： AD1S400A512M3

Product Specification： DDR-400(CL3) 200-Pin SO-DIMM
512MB (64M x 64-bits)

Issuing Date： 2010/07/07

Version： 0

Item：

Approval By	Write By
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Revision History

Revision	Month	Year	History
0	July	2010	- Initial Release

AD1S400A512M3
DDR-400(CL3) 200-Pin SO-DIMM
512MB (64M x 64-bits)

1. General Description：

The ADATA's module is a 64Mx64 bits 512MB DDR-400(CL3)-3-3-8 SDRAM memory module. The SPD is programmed to JEDEC standard latency 400Mbps timing of 3-3-3-8 at 2.6V. The module is composed of eight 64Mx8 bits CMOS DDR SDRAMs in TSOP 66pin package and one 2Kbit EEPROM in 8pin TSSOP (TSOP) package on a 200pin glass–epoxy printed circuit board.

The module is a Dual In-line Memory Module and intended for mounting onto 200-pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

2. Features：

- Power supply (Normal): VDD & VDDQ = 2.6V ± 0.1V
- All inputs and outputs are compatible with SSTL_2 interface
- Programmable Read latency : DDR400(3 Clock)
- Programmable Burst Length (2, 4, 8) with both sequential and interleave mode
- Programmable Burst type (sequential & interleave)
- Differential clock input (CK, /CK)
- DLL aligns DQ and DQS transition with CK transition
- Double-data-rate architecture ; two data transfers per clock cycle
- Bidirectional data strobe [DQ] (x4,x8) & [L(U)DQS] (x16)
- Programmable Burst type (sequential & interleave)
- Auto & Self refresh, 7.8us refresh interval (8K/64ms refresh)
- Lead-free products are RoHS Compliant

3. Pin Assignment：

Front Side									Back Side							
PIN	Name	PIN	Name	PIN	Name	PIN	Name		PIN	Name	PIN	Name	PIN	Name	PIN	Name
1	VREF	51	VSS	103	VSS	155	VDD		2	VREF	52	VSS	104	VSS	156	VDD
3	VSS	53	DQ19	105	A7	157	VDD		4	VSS	54	DQ23	106	A6	158	/CK1
5	DQ0	55	DQ24	107	A5	159	VSS		6	DQ4	56	DQ28	108	A4	160	/CK1
7	DQ1	57	VDD	109	A3	161	VSS		8	DQ5	58	VDD	110	A2	162	VSS
9	VDD	59	DQ25	111	A1	163	DQ48		10	VDD	60	DQ29	112	A0	164	DQ52
11	DQS0	61	DQS3	113	VDD	165	/DQ49		12	DM0	62	DM3	114	VDD	166	DQ53
13	DQ2	63	VSS	115	A10/AP	167	VDD		14	DQ6	64	VSS	116	BA1	168	VDD
15	VSS	65	DQ26	117	BA0	169	DQS6		16	VSS	66	DQ30	118	/RAS	170	DM6
17	DQ3	67	DQ27	119	/WE	171	DQ50		18	DQ7	68	DQ31	120	/CAS	172	DQ54
19	DQ8	69	VDD	121	/CS0	173	VSS		20	DQ12	70	VDD	122	/CS1	174	VSS
21	VDD	71	CB0	123	DU	175	DQ51		22	VDD	72	CB4	124	DU	176	DQ55
23	DQ9	73	CB1	125	VSS	177	DQ56		24	DQ13	74	CB5	126	VSS	178	DQ60
25	DQS1	75	VSS	127	DQ32	179	VDD		26	DM1	76	VSS	128	DQ36	180	VDD
27	VSS	77	DQS8	129	DQ33	181	DQ57		28	VSS	78	DM8	130	DQ37	182	DQ61
29	DQ10	79	CB2	131	VDD	183	DQS7		30	DQ14	80	CB6	132	VDD	184	DM7
31	DQ11	81	VDD	133	DQS4	185	VSS		32	DQ15	82	VDD	134	DM4	186	VSS
33	VDD	83	CB3	135	DQ34	187	DQ58		34	VDD	84	CB7	136	DQ38	188	DQ62
35	CK0	85	DU	137	VSS	189	DQ59		36	VDD	86	*DU/(RESET)	138	VSS	190	DQ63
37	/CK0	87	VSS	139	DQ35	191	VDD		38	VSS	88	VSS	140	DQ39	192	VDD
39	VSS	89	CK2	141	DQ40	193	SDA		40	VSS	90	VSS	142	DQ44	194	SA0
KEY		91	/CK2	143	VDD	195	SCL		KEY		92	VDD	144	VDD	196	SA1
41	DQ16	93	VDD	145	DQ41	197	VDDSPD		42	DQ20	94	VDD	146	DQ45	198	SA2
43	DQ17	95	CKE1	147	DQS5	199	VDDID		44	DQ21	96	/CKE0	148	DM5	200	DU
45	VDD	97	DU	149	VSS				46	VDD	98	*DU(BA2)	150	VSS		
47	DQS2	99	A12	151	DQ42				48	DM2	100	A11	152	DQ46		
49	DQ18	101	A9	153	DQ43				50	DQ22	102	A8	154	DQ47		

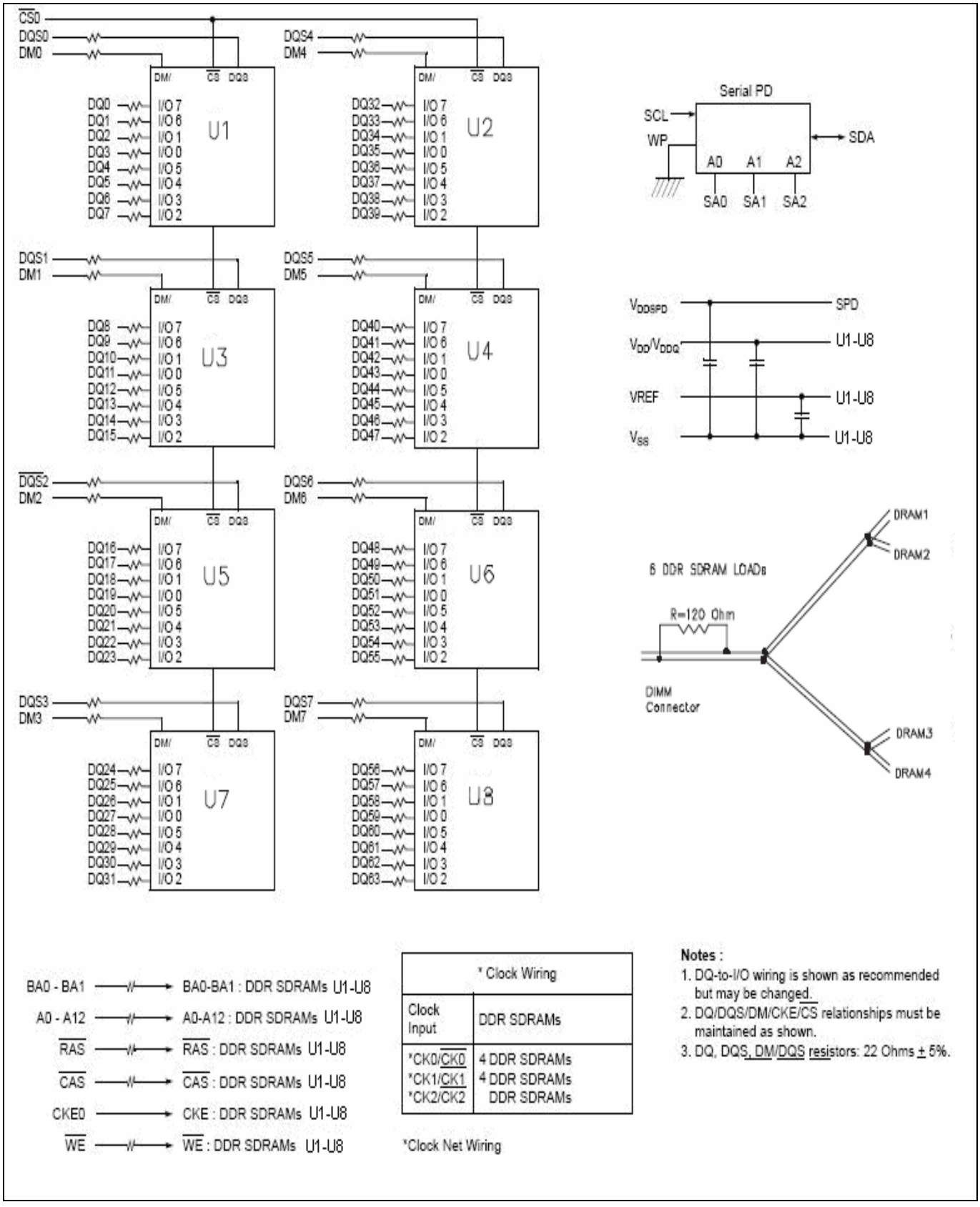
Note :1. * : These pins are not used in this module.

2. Pins 71, 72, 73, 74, 77, 78, 79, 80, 83, 84 are not used on x64(M470~) module, & used on x72(M485 ~) module.

4. Pin Description：

PIN	NAME	FUNCTION
A0~A12	Address	Row / Column address are multiplexed on the same pins.
BA0~BA1	Banks Select	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
DQ0~DQ63	Data	Data inputs / outputs are multiplexed on the same pins.
DQS0~DQS8	Data Strobe	Bi-directional Data Strobe
CK0~CK2	System Clock	Clock Inputs.
/CK0 ~ /CK2	System Clock	Differential clock inputs
CKE0,CKE1(for 2 rank)	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least on cycle prior new command. Disable input buffers for power down in standby
/CS0,/CS1(for 2 rank)	Chip Select	Disables or Enables device operation by masking or enabling all input except CK, CKE and L(U)DQM
/RAS	Row Address Strobe	Latches row addresses on the positive edge of the CK with /RAS low
/CAS	Column Address Strobe	Latches Column addresses on the positive edge of the CK with /CAS low
/WE	Write Enable	Enables write operation and row recharge.
DM0~DM7,8(for ECC)	Data Mask	Mask input data when DM is high.
VDD/ VDDQ	Power Supply	Power for the input buffers and the core logic.
VSS	Power Supply	Ground for the input buffers and the core logic.
VREF	Power Supply reference	Power Supply for reference
VDDSPD	SPD Power Supply	Serial EEPROM power Supply
SDA	Serial data I/O	EEPROM serial data I/O
SCL	Serial clock	EEPROM clock input
SA0~2	Address in EEPROM	EEPROM address input
VDDID	VDD identification	VDD identification flag
NC	No Connection	This pin is recommended to be left No Connection on the device.

5. Block Diagram：



* Clock Wiring	
Clock Input	DDR SDRAMs
*CK0/CK0	4 DDR SDRAMs
*CK1/CK1	4 DDR SDRAMs
*CK2/CK2	DDR SDRAMs

*Clock Net Wiring

Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms ± 5%.

6. Absolute Maximum Ratings：

Parameter	Symbol	Value	Unit
Operating Temperature (Ambient)	TA	0 ~ 70	℃
Voltage on VDD supply relative to Vss	VDD	-1.0 ~ 3.6	V
Voltage on VDDQ supply relative to Vss	VDDQ	-1.0 ~ 3.6	V
Voltage on any pin relative to Vss	VIN, Vout	-0.5 ~ 3.6	V
Storage temperature	TSTG	-55 ~ 100	℃
Short circuit current	IOS	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

7. DC Operating Condition：

Recommended operating conditions(Voltage referenced to V_{SS}=0V, T_A=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	VDD, VDDQ	2.5	2.7	V	1
Reference voltage	VREF	VDDQ*0.49	VDDQ*0.51	V	2
Termination voltage	VTT	VREF-0.04	VREF+0.04	V	
Input logic high voltage	VIH	VREF+0.15	VDDQ+0.3	V	
Input logic low voltage	VIL	-0.3	VREF-0.15	V	3
Input voltage Level	VIN	-0.3	VDDQ+0.3	V	
Input Differential Voltage	VID	0.36	VDDQ+0.6	V	4
V-I Matching: Pullup to Pulldown current ratio	VI (ratio)	0.71	1.4	V	
Input leakage current	IL	-2	+2	uA	5
Output leakage current	IOZ	-5	5	uA	6
Output logic high voltage	VOH	VTT+0.76	-	V	IOH=-15.2mA
Output logic low voltage	VOL	-	VTT-0.76	V	IOL=15.2mA

Note : 1. VDDQ must not exceed the level of VDD.
2. The value of VREF is approximately equal to 0.5*VDDQ
3. VIL(min) is acceptable –1.5V AC pulse width with ≦ 5ns of duration.
4. VID is the magnitude of the difference between the input level on CK and the input level on /CK.
5. VIN=0 to 3.6 V, All other pins are not tested under VIN=0V
6. DQ is disabled, Vout = 0 to 2.7V

8. AC Operating Condition：

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH	VREF +0.31	-	V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL	-	VREF-0.31	V	
Input Differential Voltage, CK and /CK inputs	VID	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	VIX	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note: 1. VID is the magnitude of the difference between the input level on CK and the input level on /CK.

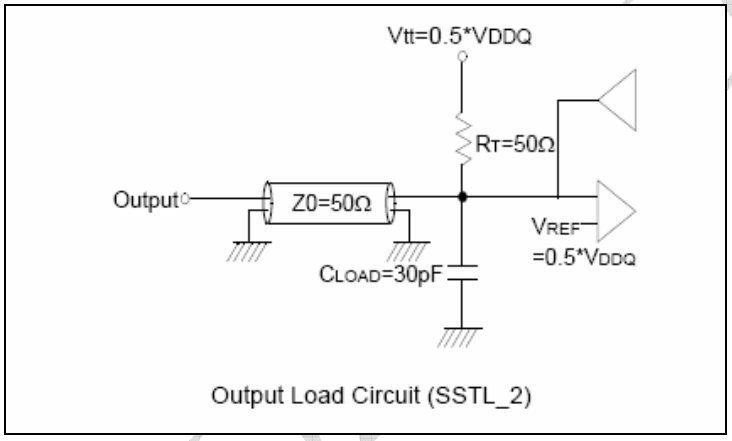
2. VIX is expected to be equal to 0.5*VDDQ of the transmitting device and must track variations in the dc level of the same.

9. AC Operation Test Condition：

(Voltage referenced to Vss = 0V, TA=0 to 70℃)

Parameter	Value	Unit
Reference Voltage	VDDQ*0.5	V
Termination Voltage	VDDQ*0.5	V
AC Input High Level Voltage (VIH, min)	VREF+0.31	V
AC Input Low Level Voltage (VIN, max)	VREF-0.31	V
Input Timing Measurement Reference Level Voltage	VREF	V
Output Timing Measurement Reference Level Voltage	VTT	V
Input Signal Maximum peak swing	1.5	V
Input signal Minimum Slew Rate	1	V/ns
Termination Resistor (RT)	50	Ohm
Series Resistor (RS)	25	Ohm
Output Load Capacitance For Access Time Measurement	30	pF

Output load circuit



Output Load Circuit (SSTL_2)

10. IDD Specification and Conditions：

(TA=0 to 70℃, Voltage referenced to Vss = 0V)

Symbol	Condition	Typical	Unit
IDD0	One bank Active-Precharge	960	mA
IDD1	One bank Active-Read-Precharge	1,200	mA
IDD2P	Precharge power-down standby current	40	mA
IDD2F	Precharge floating standby current	240	mA
IDD3P	Active power-down standby current	360	mA
IDD3N	Active standby current	480	mA
IDD4R	Operating current-burst read	1,240	mA
IDD4W	Operating current-burst write	1,400	mA
IDD5	Auto refresh current	1,760	mA
IDD6	Self refesh current	40	mA
IDD7	Operating current-Four bank operation	3,080	mA

Note : Module IDD was calculated on the basis of component IDD. Only for reference.

11. AC Characteristics：

Parameter		Symbol	Min	Max	Unit
Row cycle time		tRC	55	-	ns
Refresh row cycle time		tRFC	70	-	ns
Row active time		tRAS	40	70K	ns
/RAS to /CAS delay		tRCD	15	-	ns
/RAS to /RAS bank active delay		tRRD	10	-	ns
/RAS precharge time		tRP	15	-	ns
Write recovery time		tWR	15	-	ns
Write to Read command Delay		tWTR	2	-	tCK
Auto Precharge Write Recovery + Precharge		tDAL	(tWR/ tCK) + (tRP/ tCK)	-	tCK
System clock Cycle time	/CAS Latency =3	tCK	5	10	ns
Clock High Level Width		tCH	0.45	0.55	tCK
Clock Low Level Width		tCL	0.45	0.55	tCK
Access time form clock		tAC	-0.65	+0.65	ns
DQS out access time from CK /CK		tDQSCK	-0.55	+0.55	ns
Data strobe edge to output data edge		tDQSQ	-	+0.4	ns
Data-Out hold time from DQS		tQH	tHP - tQHS	-	ns
Clock Half Period		tHP	Min(tCH, tCL)	-	ns

Data Hold Skew Factor	tQHS	-	+0.5	ns
Data-out high-impedance window from CK, /CK	tHZ	-0.65	+0.65	ns
Data-out low-impedance window from CK, /CK	tLZ	-0.65	+0.65	ns
Address/Control input setup time (fast slew rate)	tIS	0.6	-	ns
Address/Control input hold time (fast slew rate)	tIH	0.6	-	ns
Address/Control input setup time (slow slew rate)	tIS	0.7	-	ns
Address/Control input hold time (slow slew rate)	tIH	0.7	-	ns
Input Pulse Width	tIPW	2.2	-	ns
DQS in high level width	tDQSH	0.35	-	tCK
DQS in low level width	tDQSL	0.35	-	tCK
CK to valid DQS-in	tDQSS	0.72	1.28	tCK
DQS falling edge to CK setup time	tDSS	0.2	-	tCK
DQS falling edge hold time from CK	tDSH	0.2	-	tCK
DQ & DM input setup time	tDS	0.4	-	ns
DQ & DM input hold time	tDH	0.4	-	ns
DQ & DM Input Pulse Width	tDIPW	1.75	-	ns
Read DQS Preamable Time	tRPRE	0.9	1.1	tCK
Read DQS Postamble Time	tRPST	0.4	0.6	tCK
DQS-in setup time	tWPRES	0	-	tCK
DQS-in hold time	tWPREH	0.25	-	tCK
DQS write postamble Time	tWPST	0.4	0.6	tCK
MRS to new command	tMRD	10	-	ns
Exit Self Refresh to non-Read command	tXSNR	75	-	ns
Exit Self Refresh to Read command	tXSRD	200	-	tCK
Average Periodic Refresh Interval	tREFI	-	7.8	us

12. System Characteristics Conditions：

(The following tables are described specification parameters that required in systems using DDR devices to ensure proper performance. These characteristics are for system simulation purposes and are guaranteed by design.)

Inputs Slew Rate for DQ,DQS, and DM

Parameter	Symbol	Min	Max	Unit
DQ/DQM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC)	DCSLEW	0.5	4	V/ns

Inputs Setup & Hold Time Derating for Slew Rate

Input Slew Rate	Delta tIS	Delta tIH	Unit
0.5 V/ns	0	0	ps
0.4 V/ns	+50	0	ps
0.3 V/ns	+100	0	ps

Inputs/ Outputs Setup & Hold Time Derating for Slew Rate

Input Slew Rate	Delta tDS	Delta tDH	Unit
0.5 V/ns	0	0	ps
0.4 V/ns	+75	+75	ps
0.3 V/ns	+150	+150	ps

Inputs/ Outputs Setup & Hold Time Derating for Rise/Fall Delta Slew Rate

Input Slew Rate	Delta tDS	Delta tDH	Unit
+/-0.0 V/ns	0	0	ps
+/-0.25 V/ns	+50	+50	ps
+/-0.5 V/ns	+100	+100	ps

Output Slew Rate Characteristics(x4,x8 device only)

Slew Rate Characteristic	Typical Range	Min	Max	Unit
Pullup Slew Rate	1.2 ~ 2.5	1.0	4.5	V/ns
Pulldown Slew Rate	1.2 ~ 2.5	1.0	4.5	V/ns

Output Slew Rate Characteristics(x16 device)

Slew Rate Characteristic	Typical Range	Min	Max	Unit
Pullup Slew Rate	1.2 ~ 2.5	0.7	5.0	V/ns
Pulldown Slew Rate	1.2 ~ 2.5	0.7	5.0	V/ns

13. Command Truth-Table：

Command		CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	ADDR	A10/AP	BA
Mode Register Set		H	X	L	L	L	L	OP code		
No Operation		H	X	L	H	H	H	X		
Bank Active		H	X	L	L	H	H	RA		V
Read		H	X	L	H	L	H	CA	L	V
Read with Auto Precharge									H	
Write		H	X	L	H	L	L	CA	L	V
Write with Auto Precharge									H	
Precharge All Bank		H	X	L	L	H	L	X	H	X
Precharge select Bank									L	V
Burst Stop		H	X	L	H	H	L	X		
Auto Refresh		H	H	L	L	L	H	X		
Self Refresh	Entry	H	L	L	L	L	H	X		
	Exit	L	H	L	H	H	H			
				H	X	X	X			
Precharge Power down	Entry	H	L	H	X	X	X	X		
				L	H	H	H			
	Exit	L	H	H	X	X	X			
				L	V	V	V			
Active Power Down	Entry	H	L	H	X	X	X	X		
				L	V	V	V			
	Exit	L	H	X	X	X	X			

14. Package Dimensions：