

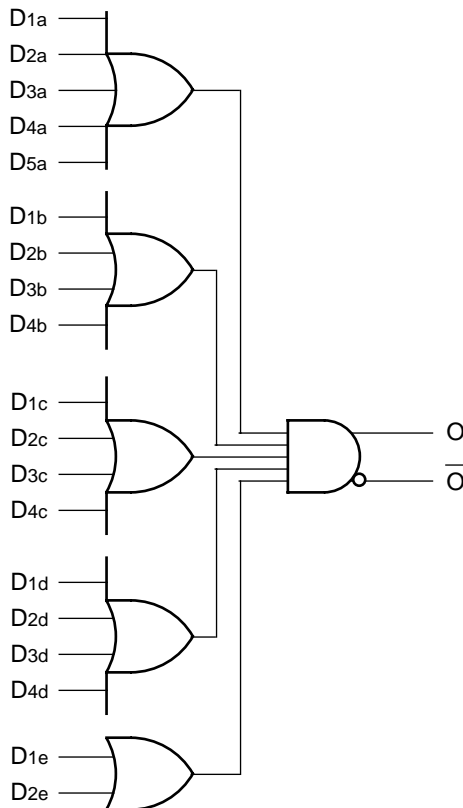
**FEATURES**

- Max. propagation delay of 800ps
- IEE min. of -55mA
- Extended supply voltage option:  
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75kΩ input pull-down resistors
- 70% faster than Fairchild
- 40% lower power than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

**DESCRIPTION**

The SY100S318 is an ultra-fast 5-wide 5, 4, 4, 4, 2 OR/AND gate with both true and complementary outputs, designed for use in high-performance ECL systems. The inputs on this device have 75kΩ pull-down resistors.

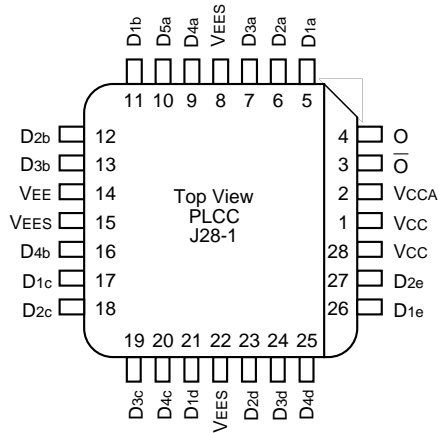
**BLOCK DIAGRAM**



**PIN NAMES**

Pin	Function
D <sub>na</sub> – D <sub>ne</sub>	Data Inputs (n = 1...5)
O – $\bar{O}$	Data Outputs
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

**PACKAGE/ORDERING INFORMATION**



**28-Pin PLCC (J28-1)**

**Ordering Information**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S318JC	J28-1	Commercial	SY100S318JC	Sn-Pb
SY100S318JCTR <sup>(1)</sup>	J28-1	Commercial	SY100S318JC	Sn-Pb
SY100S318JZ <sup>(2)</sup>	J28-1	Commercial	SY100S318JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S318JZTR <sup>(1, 2)</sup>	J28-1	Commercial	SY100S318JZ with Pb-Free bar-line indicator	Matte-Sn

**Notes:**

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

**LOGIC EQUATION**

$$O = (D1a + D2a + D3a + D4a + D5a) \\ (D1b + D2b + D3b + D4b) \\ (D1c + D2c + D3c + D4c) \\ (D1d + D2d + D3d + D4d) \\ (D1e + D2e)$$

**DC ELECTRICAL CHARACTERISTICS**

V<sub>EE</sub> = -4.2V to -5.5V unless otherwise specified, V<sub>CC</sub> = V<sub>CCA</sub> = GND

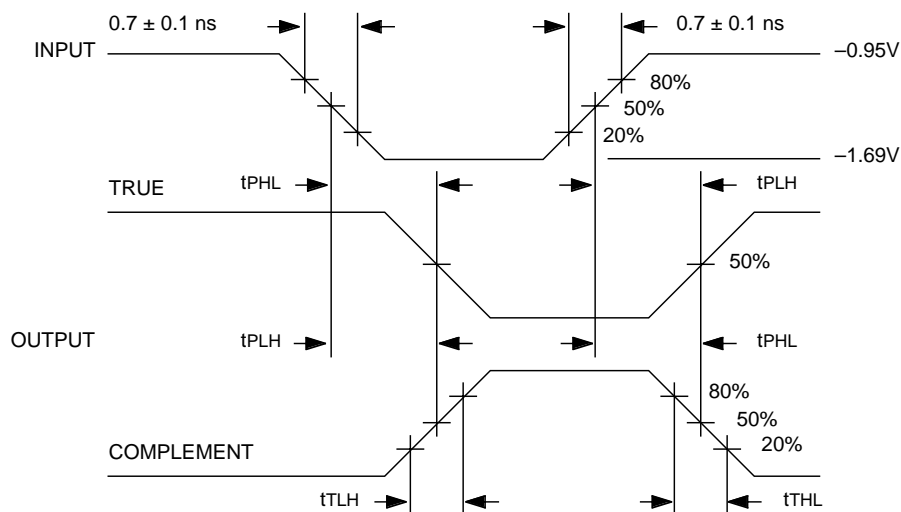
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I <sub>IH</sub>	Input HIGH Current, All Inputs	—	—	200	μA	V <sub>IN</sub> = V <sub>IH</sub> (Max.)
I <sub>EE</sub>	Power Supply Current	-55	-41	-25	mA	Inputs Open

**AC ELECTRICAL CHARACTERISTICS**

V<sub>EE</sub> = -4.2V to -5.5V unless otherwise specified, V<sub>CC</sub> = V<sub>CCA</sub> = GND

Symbol	Parameter	T <sub>A</sub> = 0°C		T <sub>A</sub> = +25°C		T <sub>A</sub> = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Data to Output	300	800	300	800	300	800	ps	
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time 20% to 80%, 80% to 20%	200	900	200	900	200	900	ps	

**TIMING DIAGRAM**

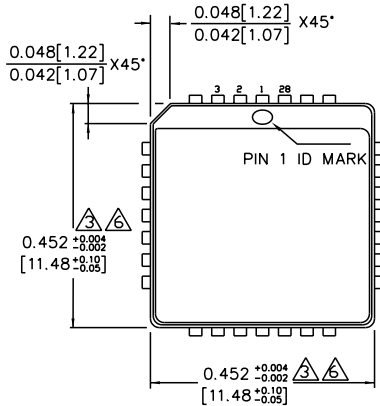


Propagation Delay and Transition Times

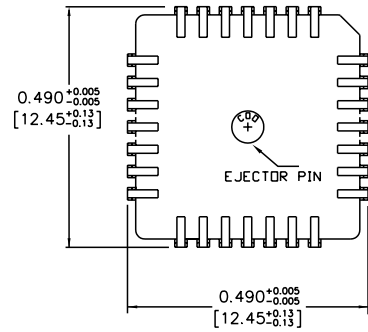
**Note:**

V<sub>EE</sub> = -4.2V to -5.5V unless otherwise specified, V<sub>CC</sub> = V<sub>CCA</sub> = GND

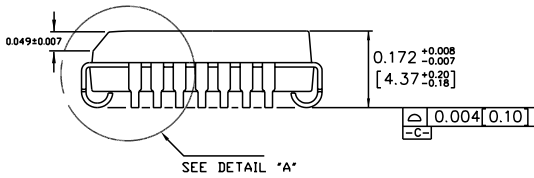
**28-PIN PLCC (J28-1)**



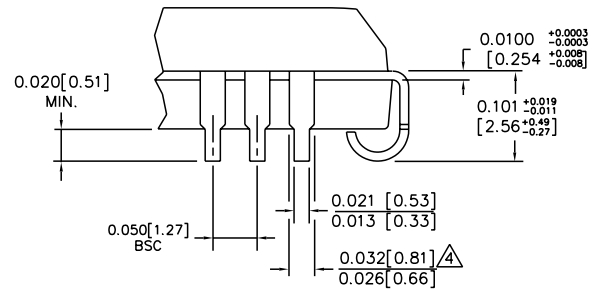
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL "A"

NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. A

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB <http://www.micrel.com>

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